

2N 5977 2N 5978 2N 5979 (SILICON) MJE5977 MJE5978 MJE5979

NPN SILICON PLASTIC POWER TRANSISTORS

... designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 5 Amperes
 $h_{FE} = 20-120 @ I_C = 2.5 \text{ Adc}$
 $= 7.0 (\text{Min}) @ I_C = 5.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 40 \text{ Vdc (Min)} - 2N5977, MJE5977$
 $= 60 \text{ Vdc (Min)} - 2N5978, MJE5978$
 $= 80 \text{ Vdc (Min)} - 2N5979, MJE5979$
- High Current Gain – Bandwidth Product
 $f_T = 2.0 \text{ MHz (Min)} @ I_C = 500 \text{ mAdc}$
- Complement to PNP Transistors –
 $2N5974, 2N5975, 2N5976 \text{ and } MJE5974, MJE5975, MJE5976$
- Choice of Packages – 2N5977 Series – Case 90
 $MJE5977 \text{ Series – Case 199}$

5 AMPERE POWER TRANSISTORS NPN SILICON 40-60-80 VOLTS 75 WATTS

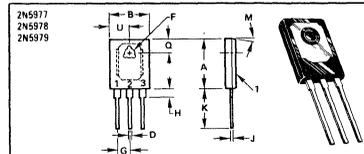
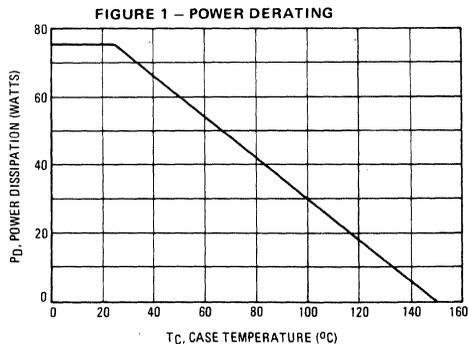
*MAXIMUM RATINGS

Rating	Symbol	2N5977 MJE5977	2N5978 MJE5978	2N5979 MJE5979	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous Peak	I_C	← 5.0 → ← 10 →			A dc
Base Current	I_B	← 2.0 →			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 75 → ← 0.60 →			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data for 2N5977 Series.

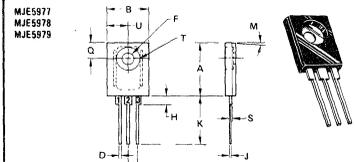


STYLE 2
PIN 1: EMITTER
2: COLLECTOR
3: BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.33	0.635	0.645
B	12.57	12.63	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.00	1.24	0.043	0.049
E	3.51	3.76	0.138	0.148
F	4.22 BSC	0.168 BSC		
G	2.67	2.92	0.105	0.115
H	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	30 TYP	30 TYP		
N	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.46	0.245	0.255

NOTE
1 LEADS WITHIN 005° RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05



STYLE 1
PIN 1: BASE
2: COLLECTOR
3: EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.63	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.91	3.86	0.142	0.152
G	2.54 BSC	0.100 BSC		
H	2.67	2.92	0.105	0.115
J	0.42	0.68	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	30 TYP	30 TYP		
N	1.47	1.73	0.058	0.068
Q	4.76	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.89	7.24	0.271	0.285
U	6.22	6.46	0.245	0.255

1 DIM "G" IS TO CENTER LINE OF LEADS

CASE 199-04

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100 \text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	40 60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 20 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 100 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 40 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CEX}	— — — — —	100 100 100 1.0 1.0	μAdc mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 2.5 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	40 20 7.0	— 120 —	—
Collector-Emitter Saturation Voltage ($I_C = 2.5 \text{ Adc}$, $I_B = 250 \text{ mAdc}$) ($I_C = 5.0 \text{ Adc}$, $I_B = 750 \text{ mAdc}$)	$V_{CE(sat)}$	— —	0.6 1.7	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $I_B = 750 \text{ mAdc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage ($I_C = 2.5 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.4	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (2) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1.0 \text{ MHz}$)	f_T	2.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	200	pF
Small-Signal Current Gain ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	20	—	—

*Indicates JEDEC Registered Data for 2N5977 Series.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

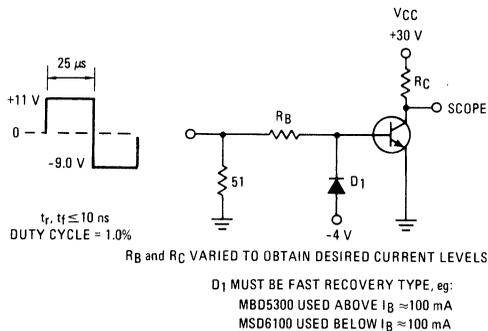


FIGURE 3 – TURN-ON TIME

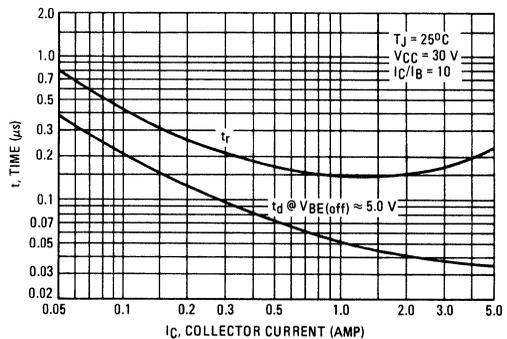


FIGURE 4 – THERMAL RESPONSE

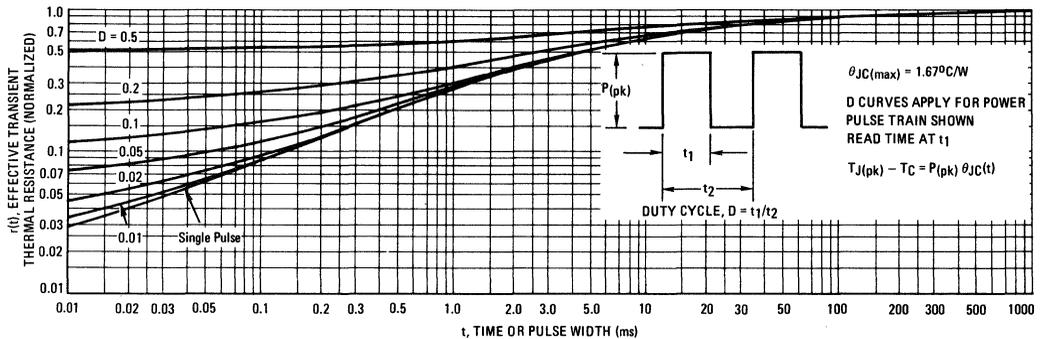
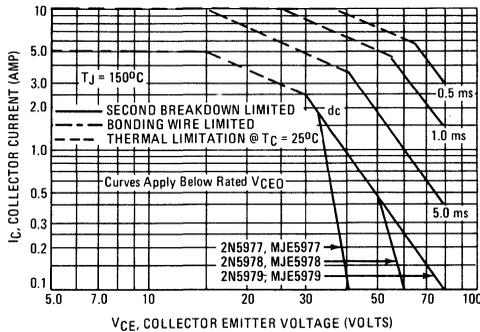


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

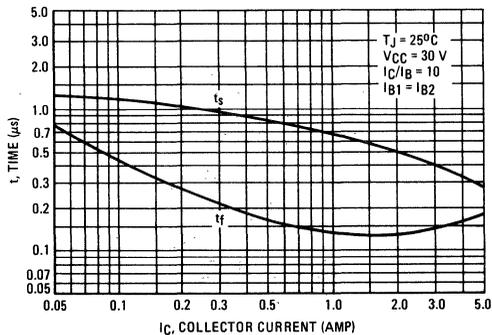


FIGURE 7 – CAPACITANCE

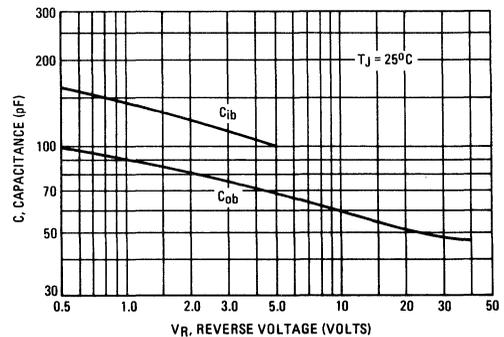


FIGURE 8 – DC CURRENT GAIN

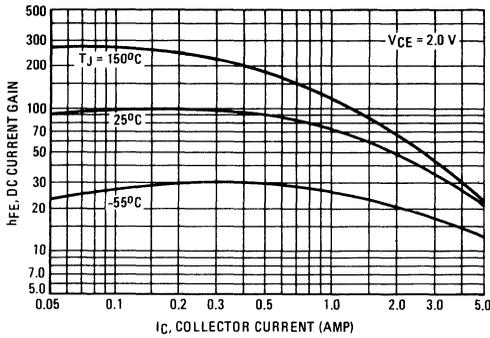


FIGURE 9 – COLLECTOR SATURATION REGION

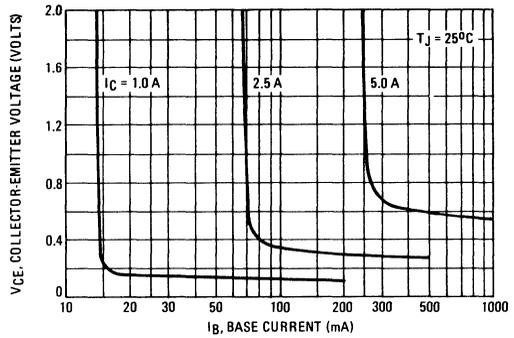


FIGURE 10 – "ON" VOLTAGES

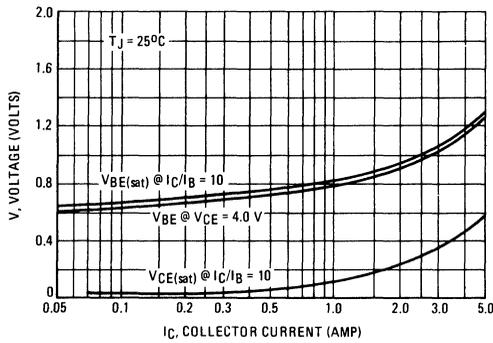


FIGURE 11 – TEMPERATURE COEFFICIENTS

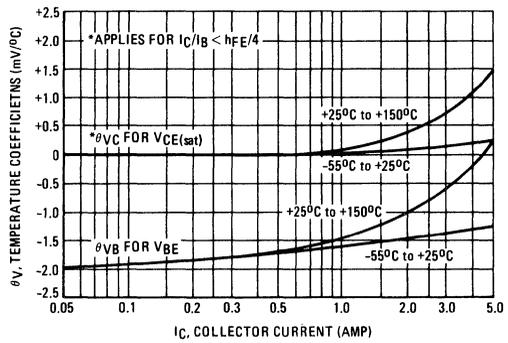


FIGURE 12 – COLLECTOR CUT-OFF REGION

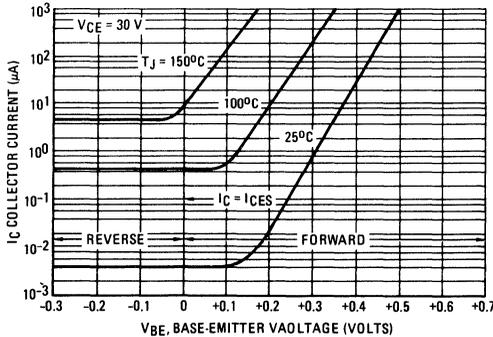


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE

