2N5986 2N5987 2N5988 PNP (SILICON)
2N5989 2N5990 2N5991 NPN

HIGH POWER PLASTIC
COMPLEMENTARY SILICON POWER TRANSISTORS

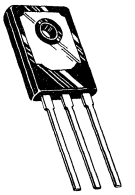
. . . designed for use in general-purpose amplifier and switching circuits.

- Collector-Base Voltage – V_{CBO} = 60 Vdc – 2N5986, 2N5989
  = 80 Vdc – 2N5987, 2N5990
  = 100 Vdc – 2N5988, 2N5991
- Collector-Emitter Voltage – V_{CEO} = 40 Vdc – 2N5986, 2N5989
  = 60 Vdc – 2N5987, 2N5990
  = 80 Vdc – 2N5988, 2N5991
- DC Current Gain –
  h_{FE} = 20-120 @ I_C = 6.0 Adc
  = 7.0 (Min) @ I_C = 12 Adc
- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 6.0 Adc

12 AMPERE

POWER TRANSISTORS
COMPLEMENTARY SILICON

40, 60, 80 VOLTS
100 WATTS



*MAXIMUM RATINGS

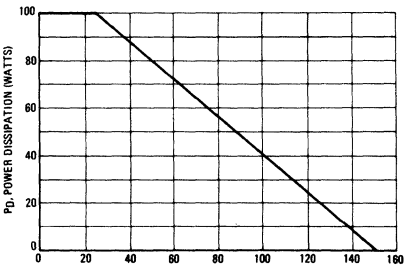
Rating	Symbol	2N5986 2N5989	2N5987 2N5990	2N5988 2N5991	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	12 20			Adc
Base Current	I_B	4.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

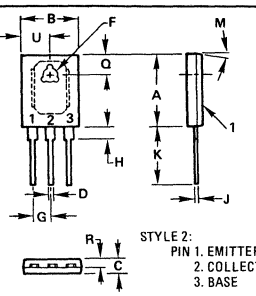
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

NOTE:
1. LEADS WITHIN .005" RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05

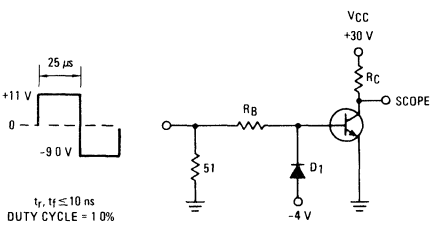
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$BV_{CEO(sus)}$			Vdc
(I_C = 0.2 Adc, I_B = 0)	2N5986, 2N5989		40	–	
	2N5987, 2N5990		60	–	
	2N5988, 2N5991		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N5986, 2N5989		–	2.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5987, 2N5990		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5988, 2N5991		–	2.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5986, 2N5989		–	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5987, 2N5990		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5988, 2N5991		–	200	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5986, 2N5989		–	2.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5987, 2N5990		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5988, 2N5991		–	2.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 12 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 6.0 Adc, I_B = 0.6 Adc)			–	0.7	
(I_C = 12 Adc, I_B = 1.8 Adc)			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 12 Adc, I_B = 1.8 Adc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)			–	1.4	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			2.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5986 thru 2N5988		–	500	
	2N5989 thru 2N5991		–	300	
Small-Signal Current Gain		h_{fe}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)			20	–	

*Indicates JEDEC Registered Data.

(1) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg.
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

For PNP test circuit reverse diode and voltage polarities.

FIGURE 3 – TURN-ON TIME

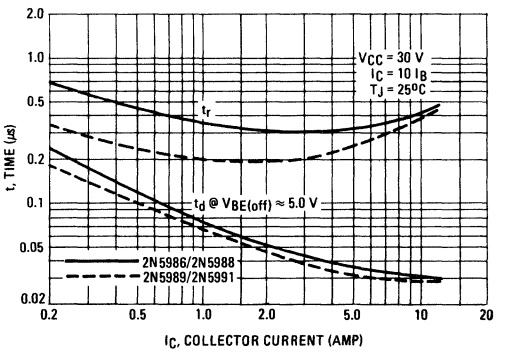


FIGURE 4 – THERMAL RESPONSE

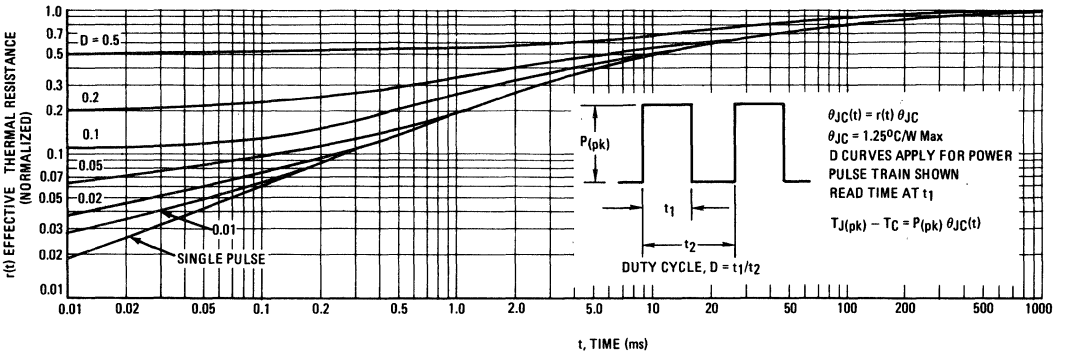
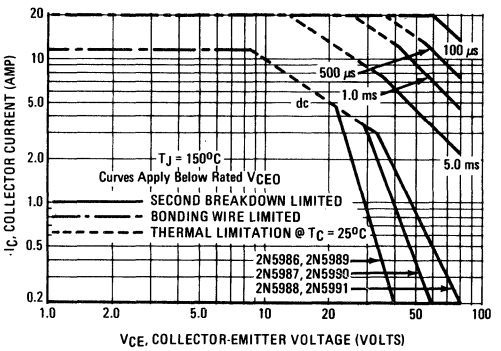


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

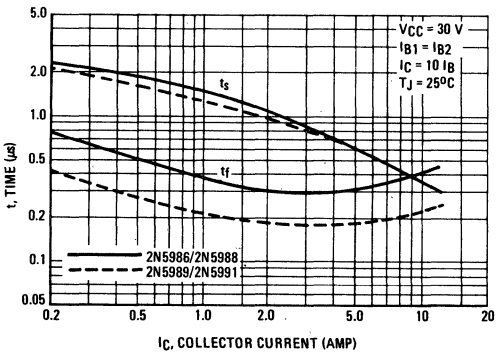
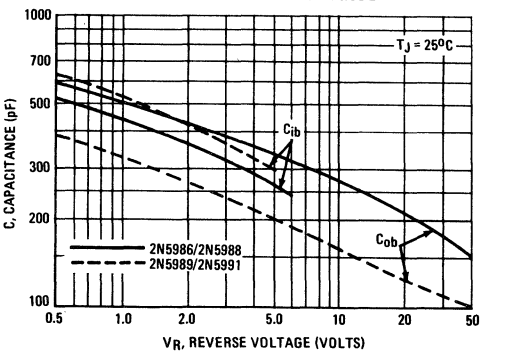


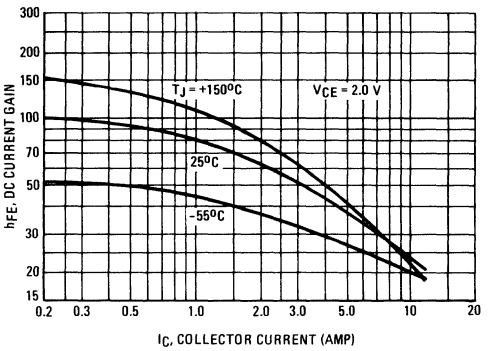
FIGURE 7 – CAPACITANCE



PNP
2N5986 thru 2N5988

NPN
2N5989 thru 2N5991

FIGURE 8 – DC CURRENT GAIN



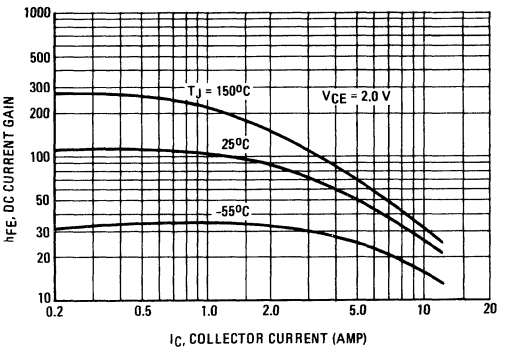
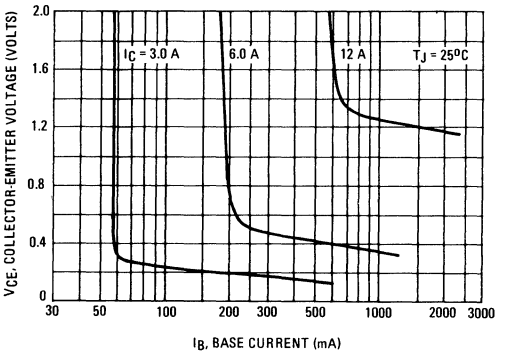


FIGURE 9 – COLLECTOR SATURATION REGION



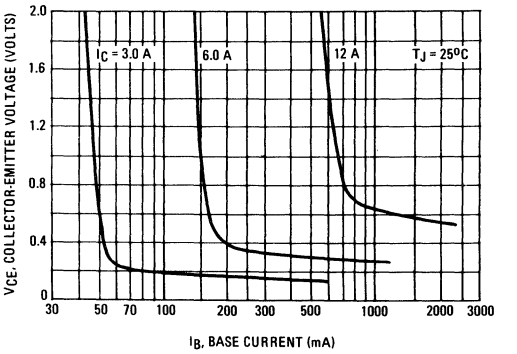
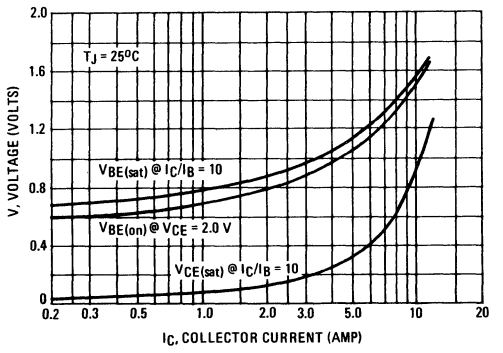
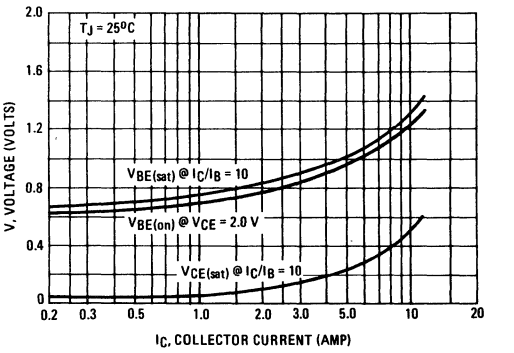


FIGURE 10 – "ON" VOLTAGES





PNP
2N5986 thru 2N5988

NPN
2N5989 thru 2N5991

FIGURE 11 – TEMPERATURE COEFFICIENTS

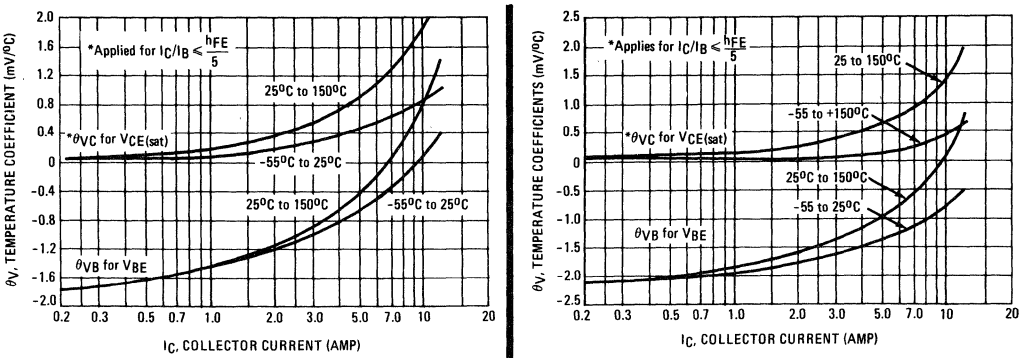


FIGURE 12 – COLLECTOR CUTOFF REGION

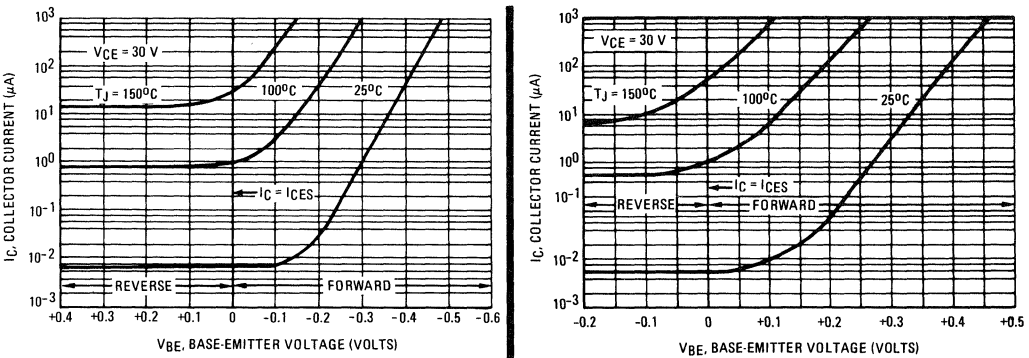


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE