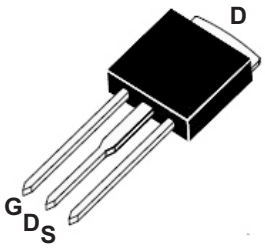
N-Channel Power MOSFET
(2A, 600Volts)

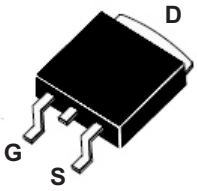
DESCRIPTION

The Nell **2N60** is a three-terminal silicon device with current conduction capability of 2A, fast switching speed, low on-state resistance, breakdown voltage rating of 600V, and max. threshold voltage of 4 volts.

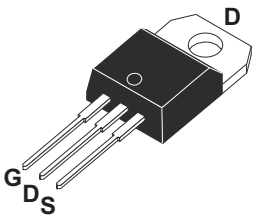
They are designed for use in applications such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits and general purpose switching applications.



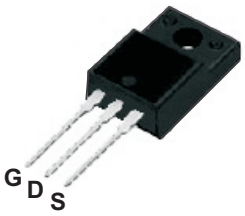
TO-251 **(I-PAK)**
(2N60F)



TO-252 **(D-PAK)**
(2N60G)



TO-220AB
(2N60A)

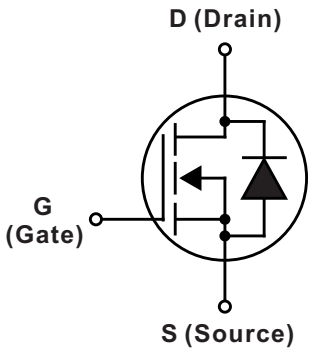


TO-220F
(2N60AF)

FEATURES

- $R_{DS(ON)}$ = 5.0Ω@V_{GS} = 10V
- Ultra low gate charge(11nC max.)
- Low reverse transfer capacitance (C_{RSS} = 5pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature

PRODUCT SUMMARY	
I_D (A)	2
V_{DSS} (V)	600
$R_{DS(ON)}$ (Ω)	5.0 @ V_{GS} = 10V
Q_G(nC) max.	11

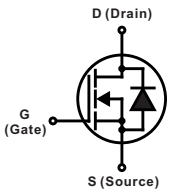


ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)					
SYMBOL	PARAMETER	TEST CONDITIONS		VALUE	UNIT
V_{DSS}	Drain to Source voltage	T_J=25°C to 150°C		600	V
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ		600	
V_{GS}	Gate to Source voltage			±30	
I_D	Continous Drain Current	T_C=25°C		2	A
		T_C=100°C		1.24	
I_{DM}	Pulsed Drain current(Note 1)			8	
I_{AR}	Avalanche current(Note 1)			2	
E_{AR}	Repetitive avalanche energy(Note 1)	I_{AR}=2A, R_{GS}=50Ω, V_{GS}=10V		4.5	mJ
E_{AS}	Single pulse avalanche energy (Note 2)	I_{AS}=2A, L = 64mH		140	
dv/dt	Peak diode recovery dv/dt(Note 3)			4.5	V /ns
P_D	Total power dissipation	T_C=25°C	TO-251/ TO-252	44	W
			TO-220AB	54	
			TO-220F	23	
T_J	Operation junction temperature			-55 to 150	°C
T_{STG}	Storage temperature			-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case		300	
	Mounting torque, #6-32 or M3 screw			10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.I_{AS} = 2A, V_{DD} = 50V, L = 64mH, R_{GS} = 25Ω, starting T_J=25°C.
3.I_{SD} ≤ 2.4A, di/dt ≤ 200A/μs, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J=25°C.

THERMAL RESISTANCE						
SYMBOL	PARAMETER		Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-251/ TO-252			2.9	°C/W
		TO-220AB			2.35	
		TO-220F			5.5	
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-251/TO-252			100	
		TO-220AB			62.5	
		TO-220F			62.5	

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{(BR)DSS}$	Drain to Source breakdown voltage	I_D=250μA,V_{GS}=0V	600			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	I_D=250μA,V_{DS}=V_{GS}		0.4		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=600V, V_{GS}=0V, T_C=25°C			10	μA
		V_{DS}=480V, V_{GS}=0V, T_C=125°C			100	
I_{GSS}	Gate to source forward leakage current	V_{GS}=30V,V_{DS}=0V			100	nA
	Gate to source forward leakage current	V_{GS}=-30V,V_{DS}=0V			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	I_D=1.0A,V_{GS}=10V		3.5	5	Ω
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS},I_D=250μA	2.0		4	V
C_{ISS}	Input capacitance	V_{DS}=25A, V_{GS}=0V, f=1MHZ		270	350	pF
C_{OSS}	Output capacitance			40	50	
C_{RSS}	Reverse transfer capacitance			5.5	7	
$t_{d(ON)}$	Turn-on delay time	V_{DD}=300V, V_{GS}=10V, I_D=2.4A, R_{GS}=25Ω (Note 1, 2)		10	30	ns
t_r	Rise time			25	60	
$t_{d(OFF)}$	Turn-off delay time			20	50	
t_f	Fall time			25	60	
Q_G	Total gate charge	V_{DD}=480V,V_{GS}=10V, I_D=2.4A (Note 1,2)		9	11	uC
Q_{GS}	Gate to source charge			1.5		
Q_{GD}	Gate to drain charge (Miller cgarge)			4.5		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 2A, V_{GS} = 0V			1.4	V
Is (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			2	A
I_{SM}	Pulsed source current				8	
t_{rr}	Reverse recovery time	I_{SD} = 2.4A, V_{GS} = 0V, dI_F/dt = 100A/μs		180		ns
Q_{rr}	Reverse recovery charge			0.7		μC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

2 N 60 A

Current rating, I_D
2 = 2A

MOSFET series
N = N-Channel

Voltage rating, V_{DS}
60 = 600V

Package type
A = TO-220AB
AF = TO-220F
F = TO-251(I-PAK)
G = TO-252(D-PAK)

■ TEST CIRCUITS AND WAVEFORMS

Fig.1A Peak diode recovery dv/dt test circuit

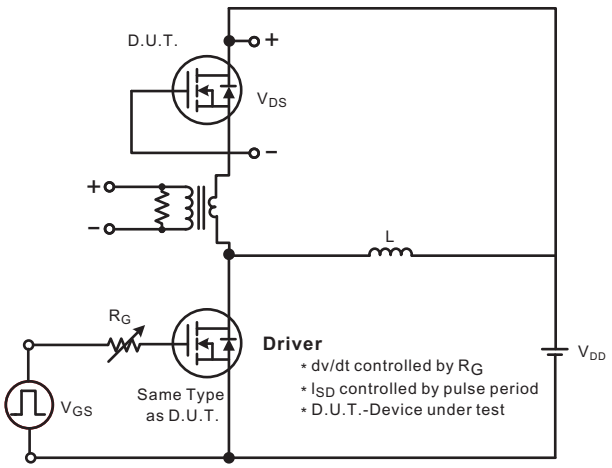
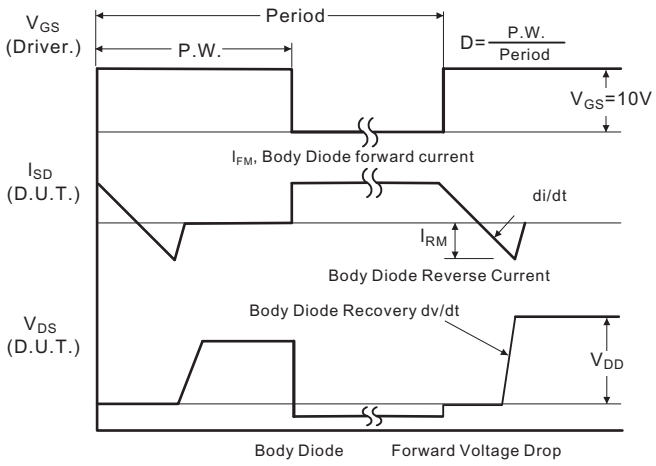


Fig.1B Peak diode recovery dv/dt waveforms



■ TEST CIRCUITS AND WAVEFORMS (Cont.)

Fig.2A Switching test circuit

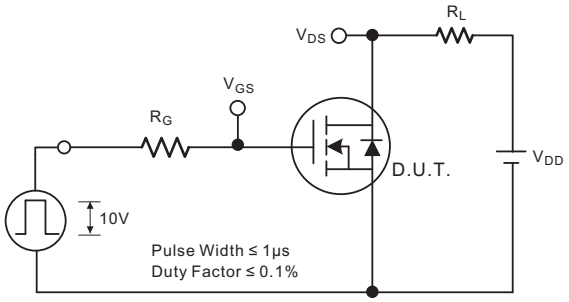


Fig.2B Switching Waveforms

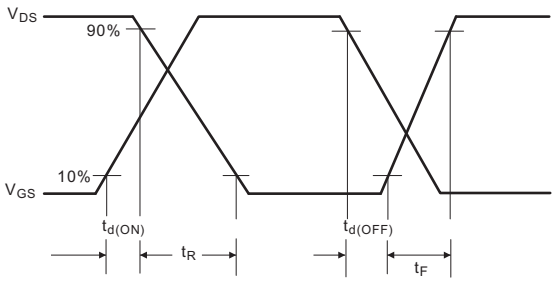


Fig.3A Gate charge test circuit

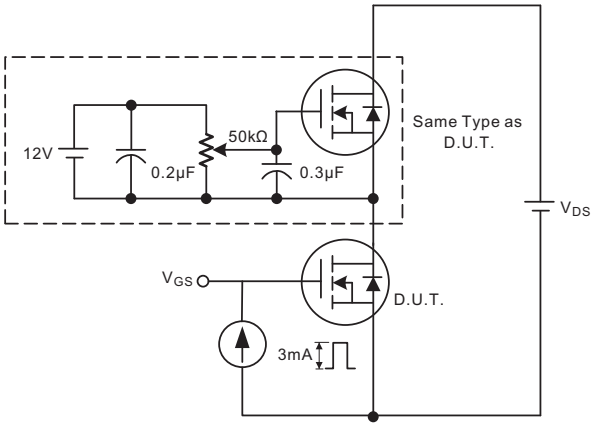


Fig.3B Gate charge waveform

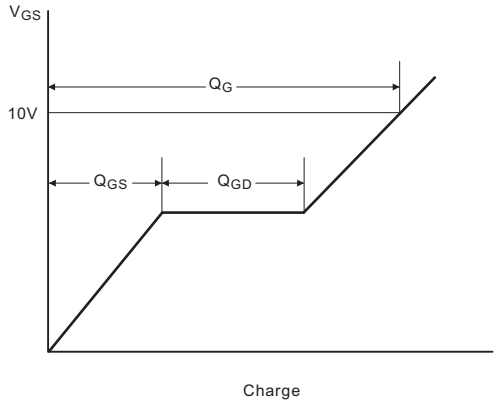


Fig.4A Unclamped Inductive switching test circuit

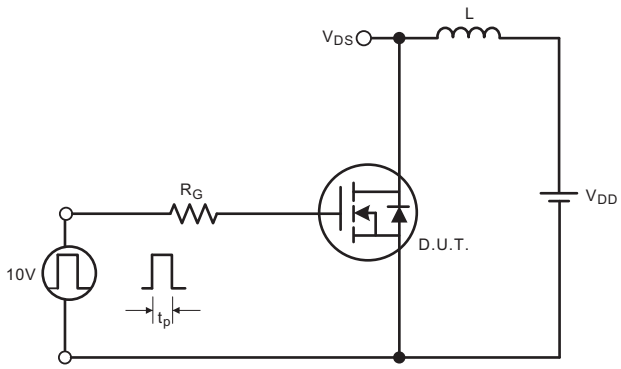
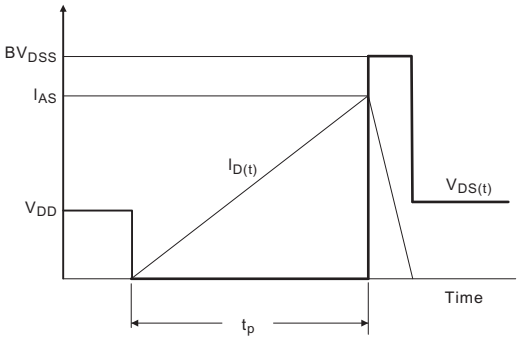


Fig.4B Unclamped Inductive switching waveforms



■ TYPICAL CHARACTERISTICS

Fig.1 Drain current vs. Drain-source breakdown voltage

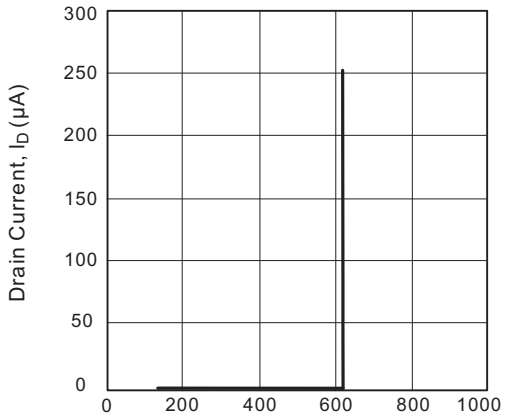


Fig.2 Drain current vs. gate threshold voltage

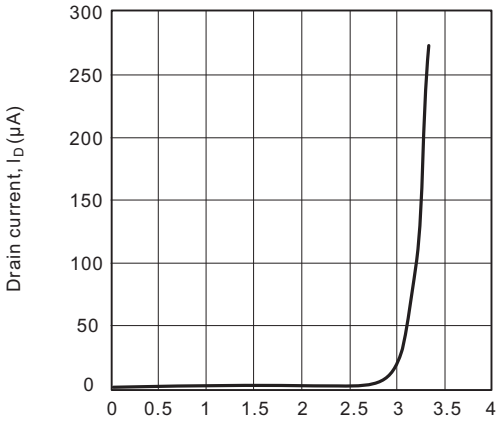


Fig.3 Drain-source on-state resistance characteristics

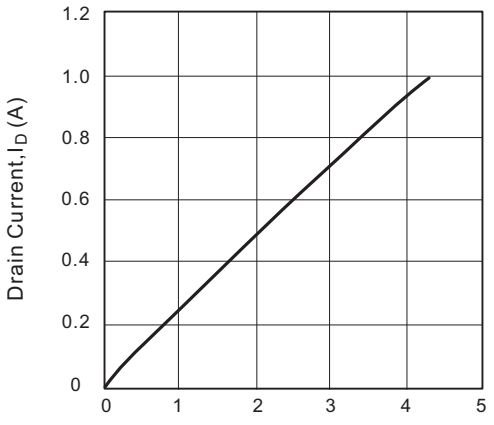
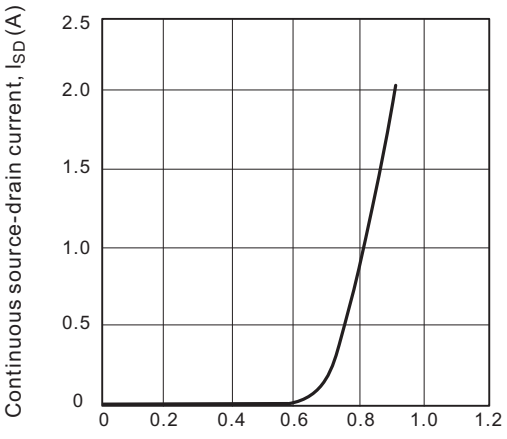
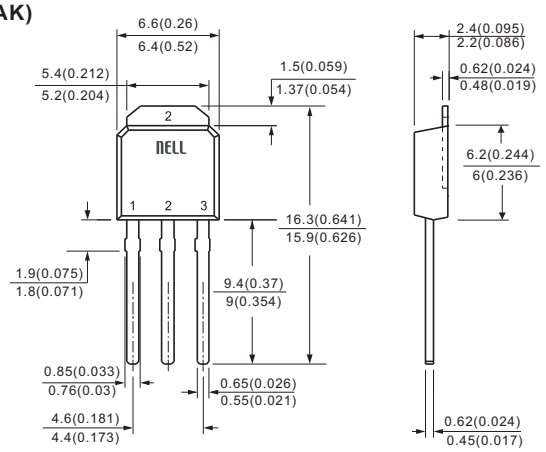


Fig.4 Drain current vs. source-drain voltage

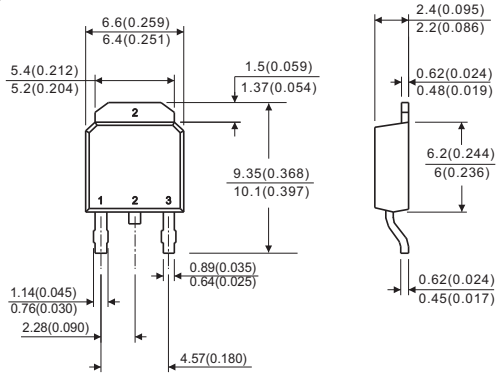


Case Style

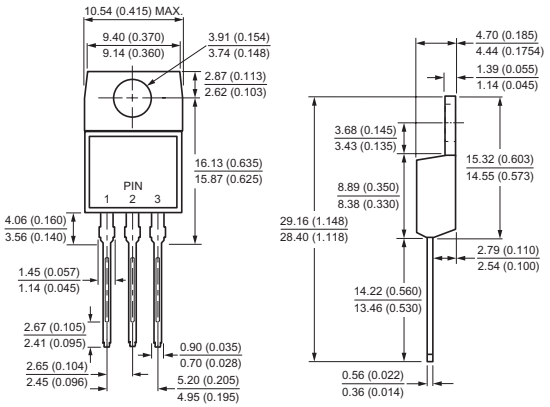
TO-251
(I-PAK)

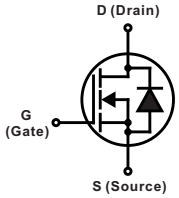


TO-252
(D-PAK)



TO-220AB

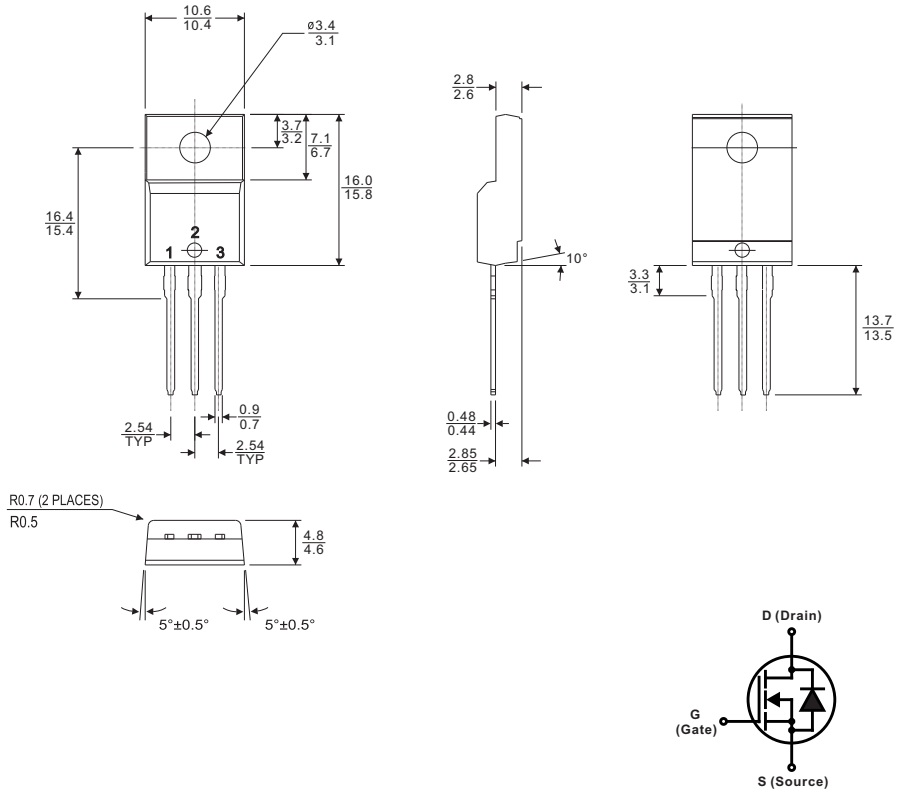




All dimensions in millimeters(inches)

Case Style

TO-220F



All dimensions in millimeters