

# High-Voltage — High Power Transistors

... designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 120 \text{ Vdc}$  — 2N5630, 2N6030  
 $= 140 \text{ Vdc}$  — 2N5631, 2N6031
- High DC Current Gain — @  $I_C = 8.0 \text{ Adc}$   
 $h_{FE} = 20 \text{ (Min)}$  — 2N5630, 2N6030  
 $= 15 \text{ (Min)}$  — 2N5631, 2N6031
- Low Collector–Emitter Saturation Voltage —  
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max)}$  @  $I_C = 10 \text{ Adc}$

## MAXIMUM RATINGS (1)

Rating	Symbol	2N5630 2N6030	2N5631 2N6031	Unit
Collector–Emitter Voltage	$V_{CEO}$	120	140	Vdc
Collector–Base Voltage	$V_{CB}$	120	140	Vdc
Emitter–Base Voltage	$V_{EB}$	7.0		Vdc
Collector Current — Continuous Peak	$I_C$	16 20		A dc
Base Current — Continuous	$I_B$	5.0		A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +200		$^\circ\text{C}$

## THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

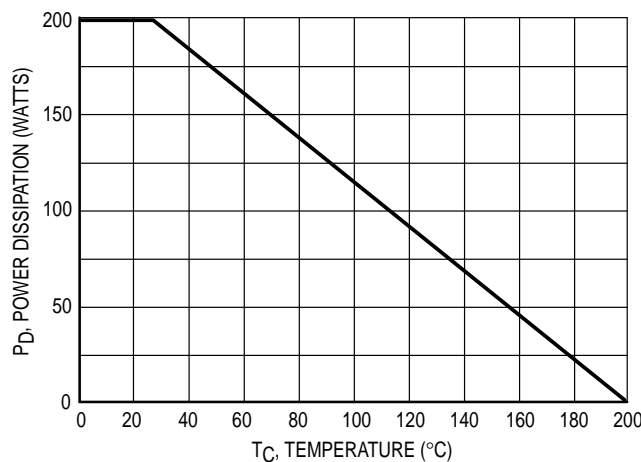


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.

**NPN**  
**2N5630**

**2N5631**  
**PNP**  
**2N6030**

**2N6031**

**16 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**100–120–140 VOLTS**  
**200 WATTS**

**CASE 1-07**  
**TO-204AA**  
**(TO-3)**

**2N5630 2N5631 2N6030 2N6031**

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 200\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	120 140	—	Vdc
Collector–Emitter Cutoff Current ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 70\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— —	2.0 2.0	mAdc
Collector–Emitter Cutoff Current ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CB}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— —	2.0 7.0	mAdc
Collector–Base Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	—	2.0	mAdc
Emitter–Base Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	5.0	mAdc

**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )  ( $I_C = 16\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$h_{FE}$	20 15 4.0	80 60 —	—
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 4.0\text{ Adc}$ )	$V_{CE(sat)}$	— —	1.0 2.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ )	$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$V_{BE(on)}$	—	1.5	Vdc

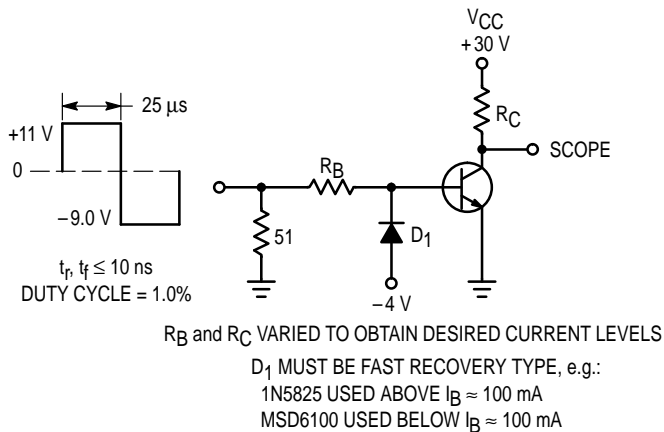
**DYNAMIC CHARACTERISTICS**

Current–Gain — Bandwidth Product (2) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 20\text{ Vdc}$ , $f_{test} = 0.5\text{ MHz}$ )	$f_T$	1.0	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	— —	500 1000	pF
Small–Signal Current Gain ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	15	—	—

\* Indicates JEDEC Registered Data.

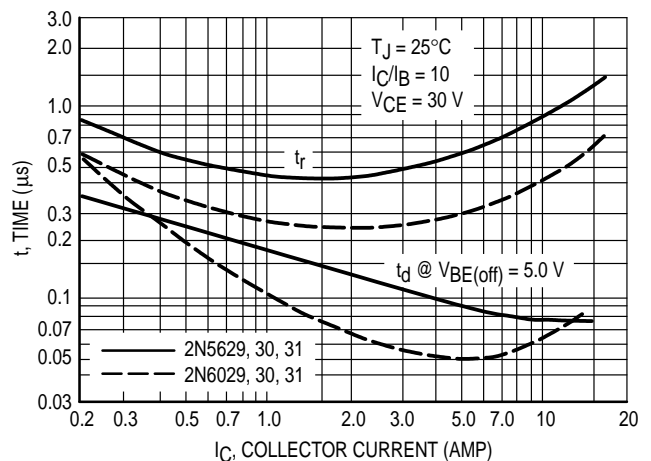
(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\geq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$



For PNP test circuit, reverse all polarities and  $D_1$ .

**Figure 2. Switching Times Test Circuit**



**Figure 3. Turn–On Time**

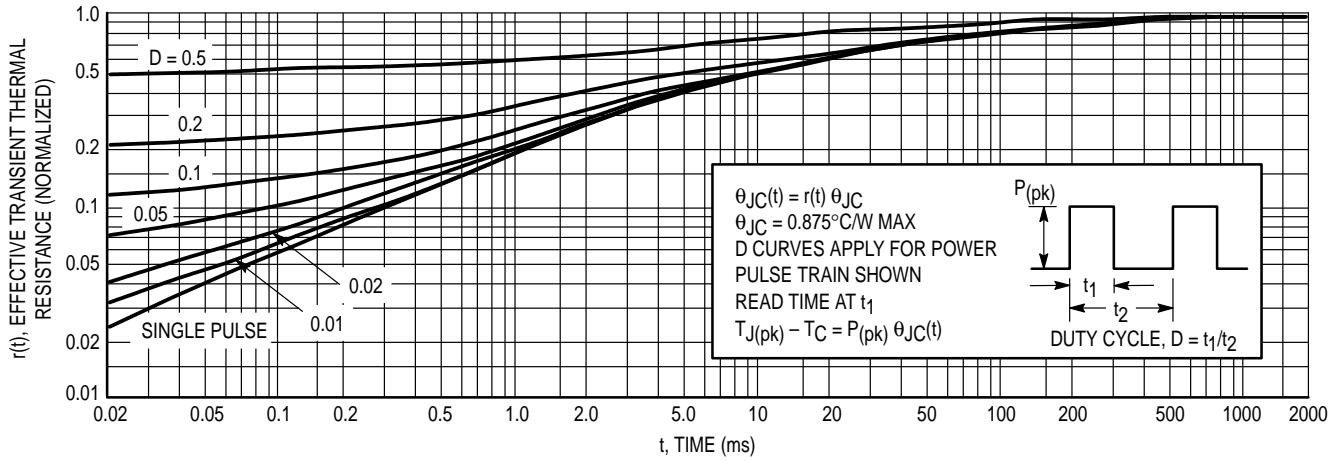


Figure 4. Thermal Response

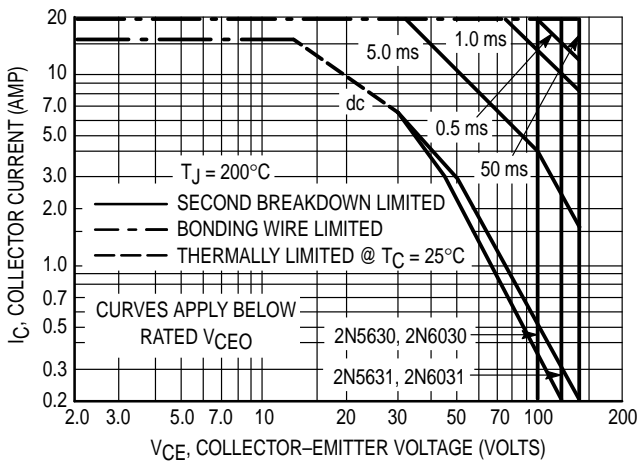


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

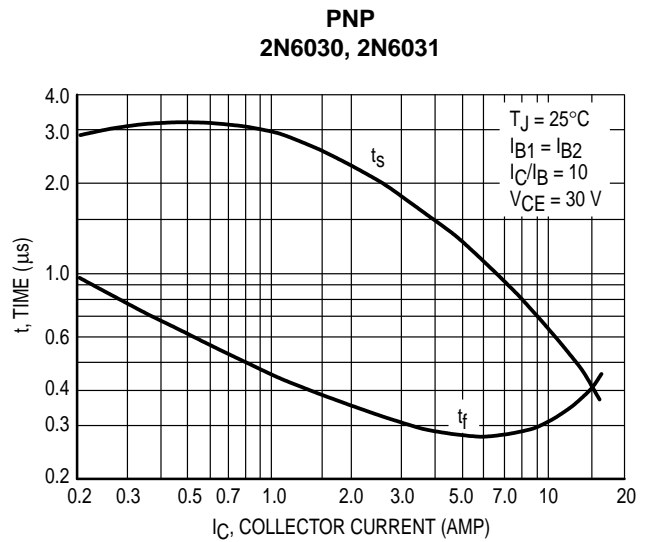
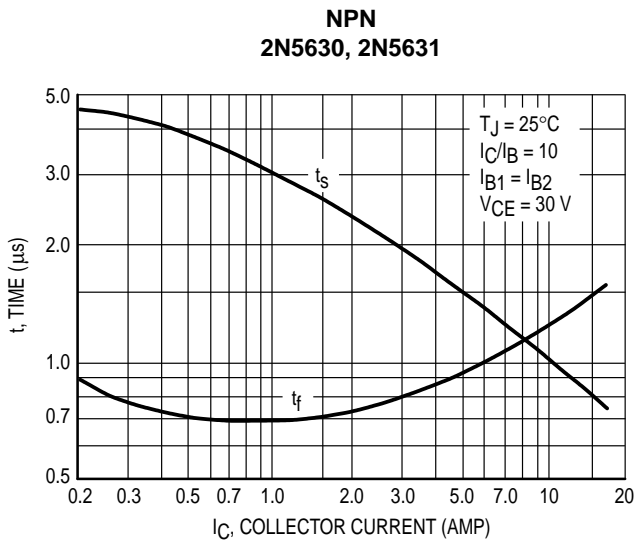
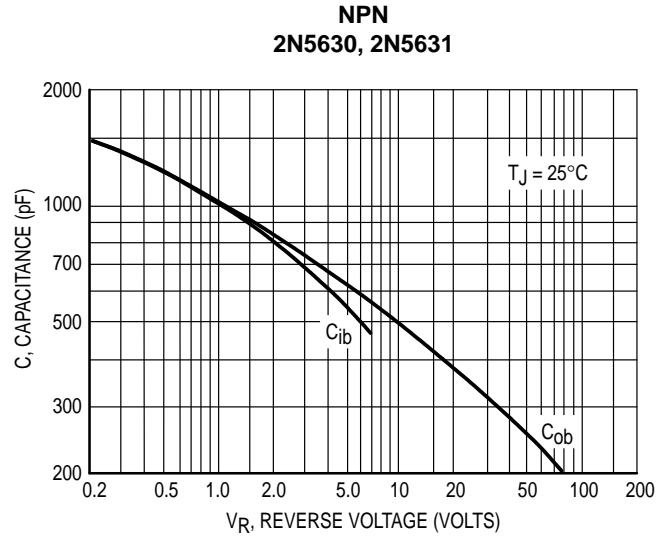
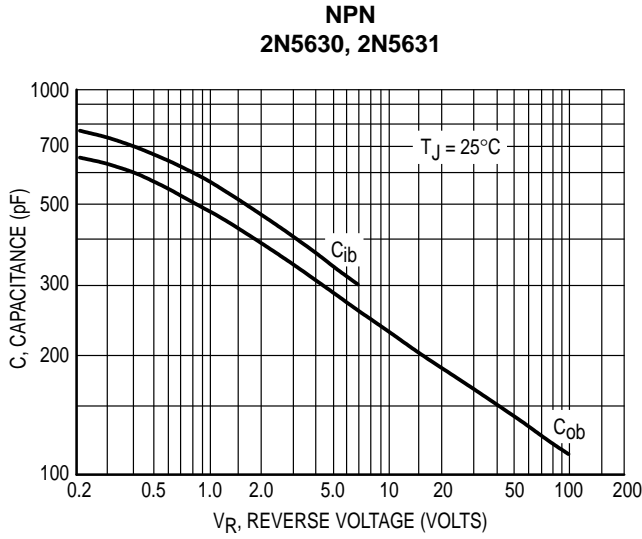
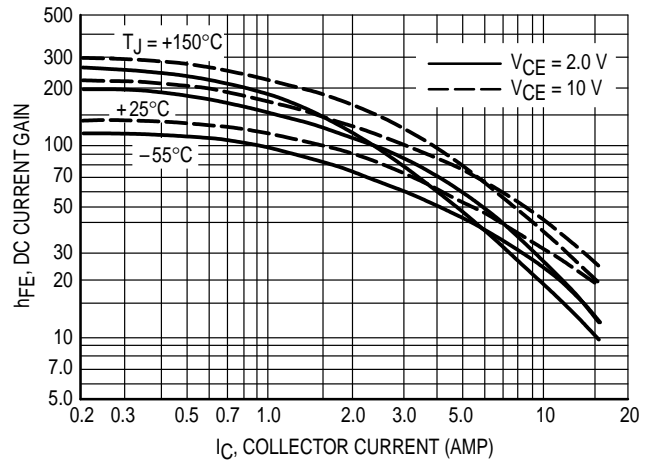
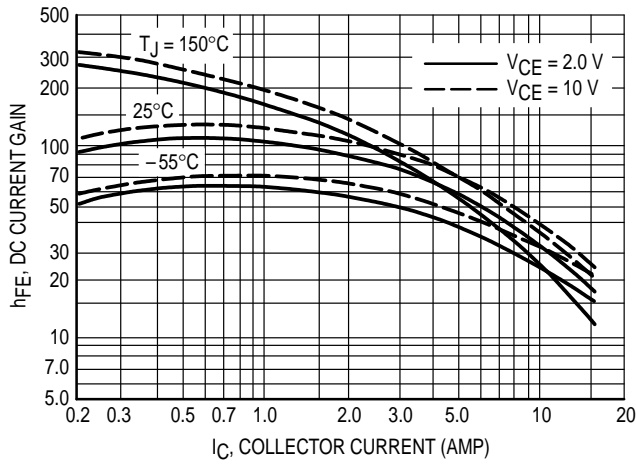


Figure 6. Turn-Off Time

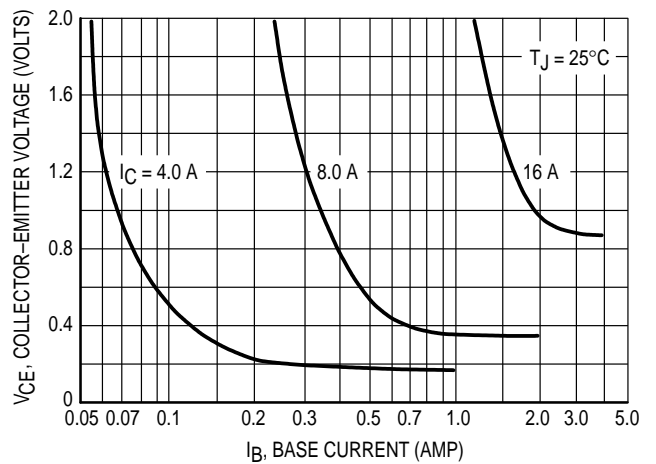
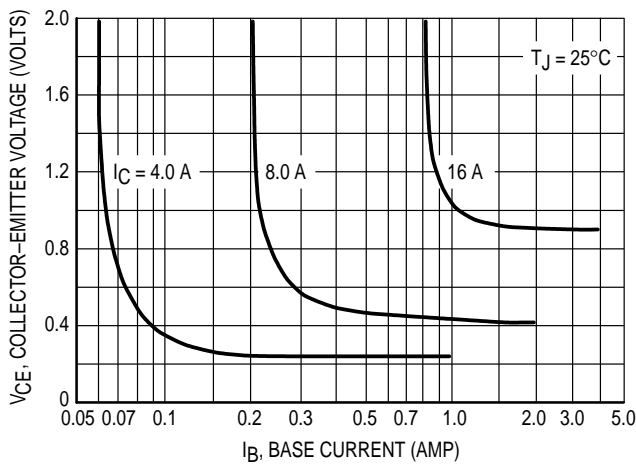
**2N5630 2N5631 2N6030 2N6031**



**Figure 7. Capacitance**

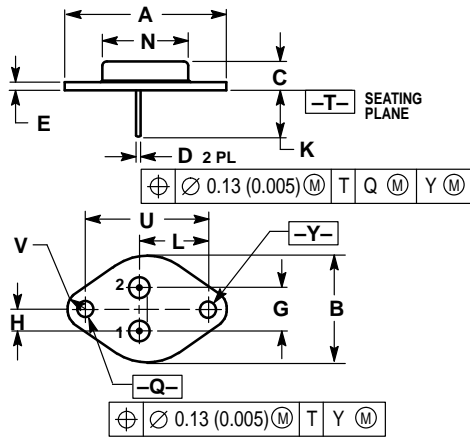


**Figure 8. DC Current Gain**



**Figure 9. Collector Saturation Region**

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:  
 PIN 1. BASE  
 2. EMITTER  
 CASE: COLLECTOR

CASE 1-07  
 TO-204AA (TO-3)  
 ISSUE Z

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