



SOLID STATE INC.

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Triacs

Silicon Bidirectional Triode Thyristors

... designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

**2N6157
thru
2N6165**

**TRIACs
30 AMPERES RMS
200 thru 600 VOLTS**



MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-------------------|-------------------|----------------------|
| *Peak Repetitive Off-State Voltage ($T_J = -65$ to $+125^\circ\text{C}$) 1/2 Sine Wave 50 to 60 Hz, Gate Open | V_{DRM} | | Volts |
| *Peak Principal Voltage 2N6157, 2N6160, 2N6163 2N6158, 2N6161, 2N6164 2N6159, 2N6162, 2N6165 | | 200 400 600 | |
| *Peak Gate Voltage | V_{GM} | 10 | Volts |
| *RMS On-State Current ($T_C = -65$ to $+85^\circ\text{C}$) ($T_C = +100^\circ\text{C}$) Full Sine Wave, 50 to 60 Hz | $I_T(\text{RMS})$ | 30 20 | Amps |
| *Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceded and followed by a 30 A RMS current, $T_J = +125^\circ\text{C}$) | I_{TSM} | 250 | Amps |
| Circuit Fusing Considerations ($T_J = -65$ to $+125^\circ\text{C}$, $t = 1$ to 8.3 ms) | I^2t | 210 | A^2s |
| *Peak Gate Power ($T_J = +80^\circ\text{C}$, Pulse Width = 2 μs) | P_{GM} | 20 | Watts |
| *Average Gate Power ($T_J = +80^\circ\text{C}$, $t = 8.3$ ms) | $P_{G(AV)}$ | 0.5 | Watt |
| *Peak Gate Current | I_{GM} | 2 | Amps |
| *Operating Junction Temperature Range | T_J | - 65 to +125 | $^\circ\text{C}$ |
| *Storage Temperature Range | T_{stg} | - 65 to +150 | $^\circ\text{C}$ |
| *Stud Torque 2N6160 thru 2N6165 | — | 30 | in. lb. |

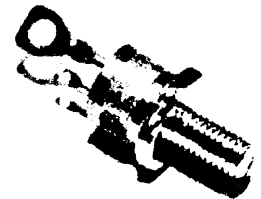
THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---------------------------------------|-----------------|-----|---------------------------|
| *Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 1 | $^\circ\text{C}/\text{W}$ |

*Indicates JEDEC Registered Data.



2N6157
2N6158
2N6159



2N6160
2N6161
2N6162



2N6163
2N6164
2N6165

2N6157 thru 2N6165

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------------------|-------------------------|---------------------------|-------------------------------|------------------------------|
| *Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ | I_{DRM}, I_{RRM} | — — | — — | 10 2 | μA mA |
| *Peak On-State Voltage (Either Direction) ($I_{TM} = 42\text{ A Peak}$, Pulse Width = 1 to 2 ms, Duty Cycle $\leq 2\%$) | V_{TM} | — | 1.5 | 2 | Volts |
| Gate Trigger Current (Continuous dc), Note 1 (Main Terminal Voltage = 12 Vdc, $R_L = 50\text{ Ohms}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+) *MT2(+), G(+); MT2(-), G(-) $T_C = -65^\circ\text{C}$ *MT2(+), G(-); MT2(-), G(+), $T_C = -65^\circ\text{C}$ | I_{GT} | — — — — — | 15 20 20 30 | 60 70 70 100 | mA |
| Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, $R_L = 50\text{ Ohms}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+) *All Quadrants, $T_C = -65^\circ\text{C}$ *Main Terminal Voltage = Rated V_{DRM} , $R_L = 10\text{ k ohms}$, $T_J = +125^\circ\text{C}$ | V_{GT} | — — — — 0.2 | 0.8 0.7 0.85 1.1 | 2 2.1 2.1 2.5 3.4 | Volts |
| Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open) (Initiating Current = 500 mA) MT2(+) MT2(-) *Either Direction, $T_C = -65^\circ\text{C}$ | I_H | — — — | 8 10 | 70 80 200 | mA |
| *Turn-On Time (Main Terminal Voltage = Rated V_{DRM} , $I_{TM} = 42\text{ A}$, Gate Source Voltage = 12 V, $R_S = 50\text{ Ohms}$, Rise Time = 0.1 μs , Pulse Width = 2 μs) | t_{gt} | — | 1 | 2 | μs |
| Blocking Voltage Application Rate at Commutation, $f = 60\text{ Hz}$, $T_C = 85^\circ\text{C}$ On-State Conditions: ($I_{TM} = 42\text{ A}$, Pulse Width = 4 ms, $di/dt = 17.5\text{ A/ms}$) Off-State Conditions: (Main Terminal Voltage = Rated V_{DRM} (200 μs min), Gate Source Voltage = 0 V, $R_S = 50\ \Omega$) | $dv/dt(c)$ | — | 5 | — | $\text{V}/\mu\text{s}$ |

*Indicates JEDEC Registered Data.

Note 1. All voltage polarities referenced to main terminal 1.

FIGURE 1 – RMS CURRENT DERATING

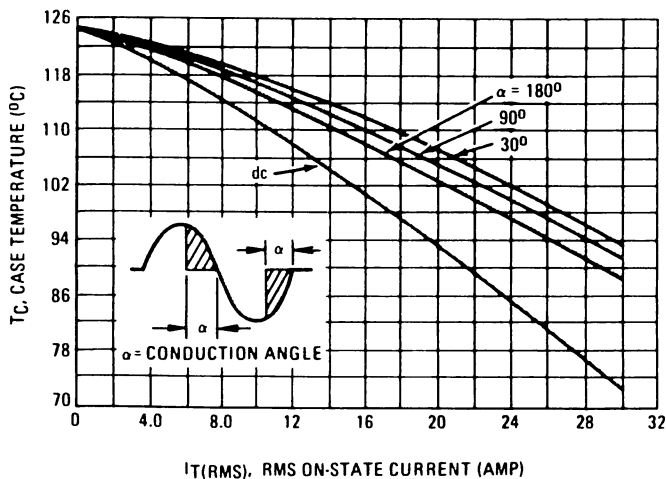


FIGURE 2 – POWER DISSIPATION

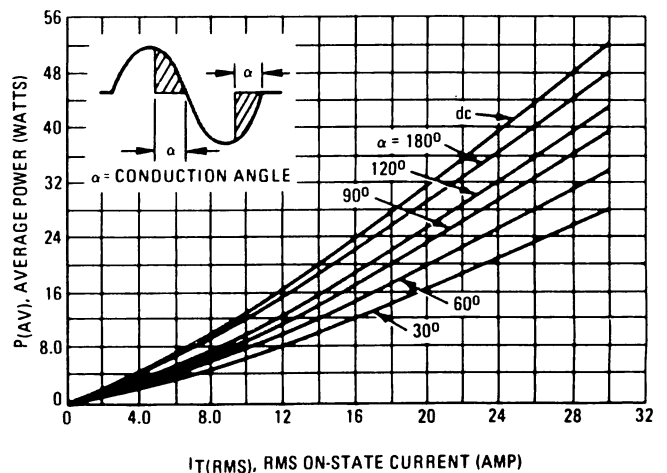


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

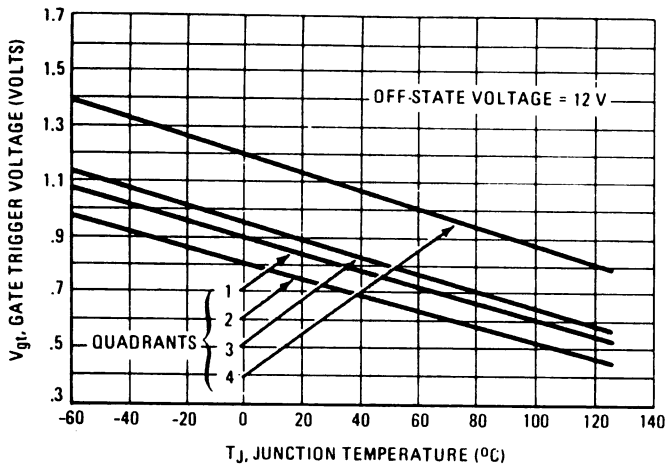


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

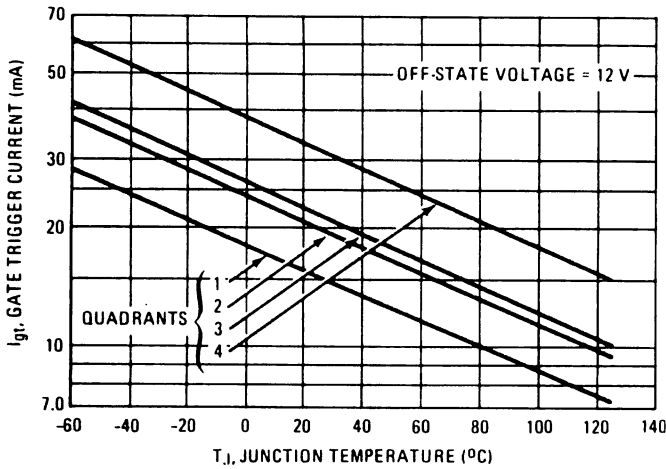


FIGURE 6 – TYPICAL HOLDING CURRENT

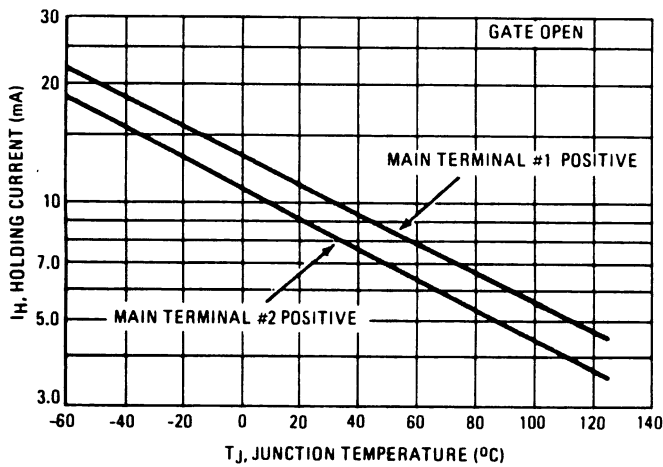


FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

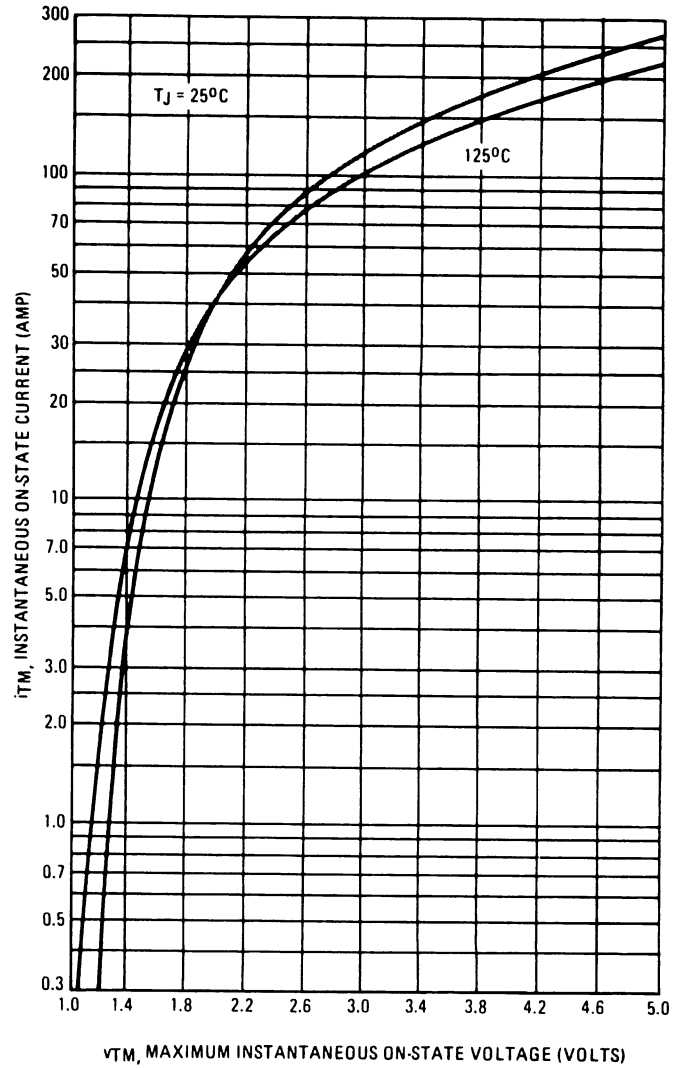
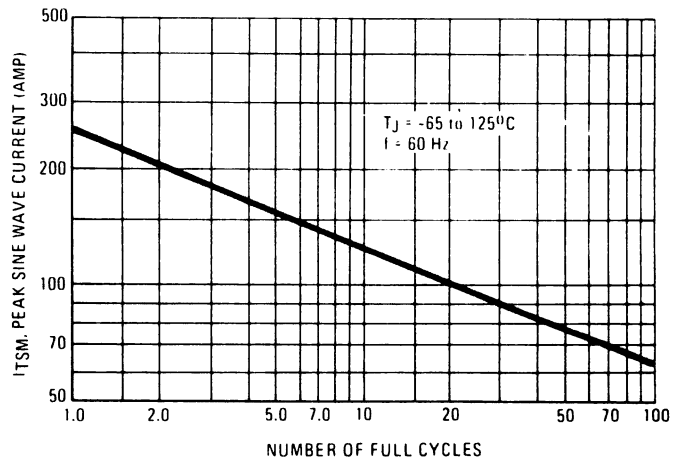
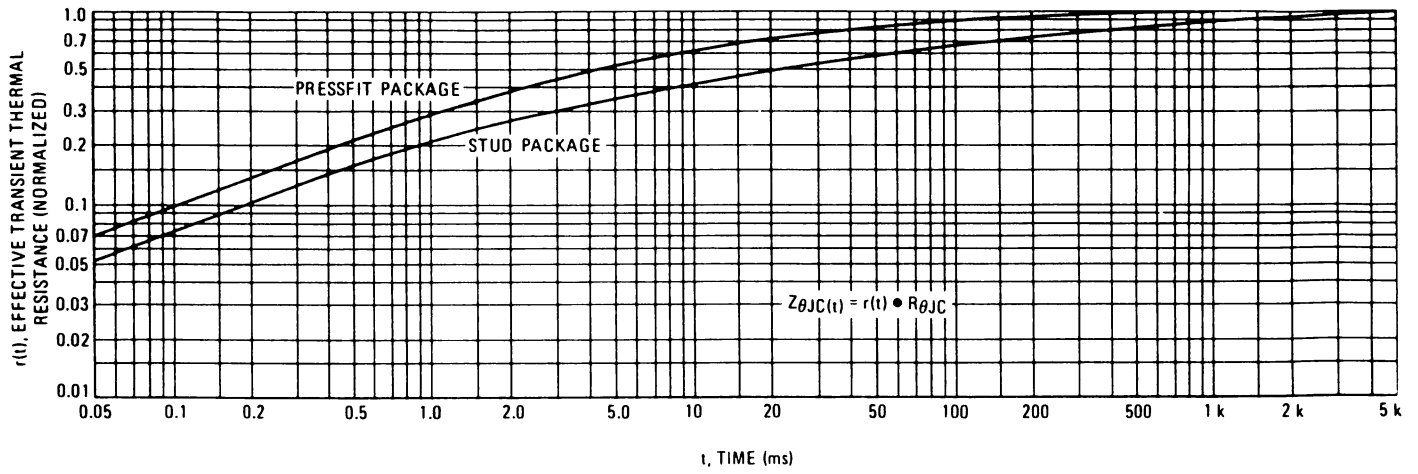


FIGURE 7 – MAXIMUM ALLOWABLE SURGE CURRENT

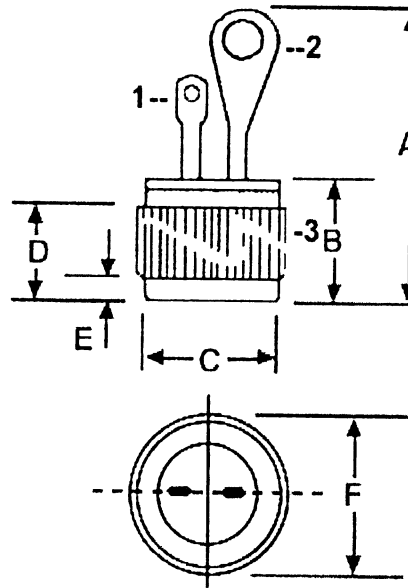


2N6157 thru 2N6165

FIGURE 8 – TYPICAL THERMAL RESPONSE



PRESS FIT TRIAC

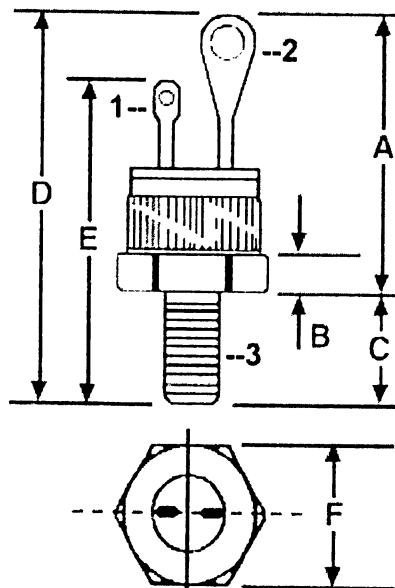
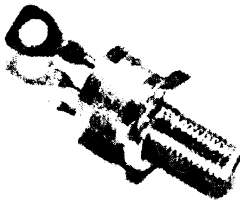


- 1. GATE
- 2. MT-1
- 3. MT-2 (case)

| SYM. | INCHES | |
|------|--------|-------|
| A | 1.050 | |
| B | 0.380 | 0.355 |
| C | 0.475 | 0.467 |
| D | 0.305 | 0.265 |
| E | 0.100 | 0.075 |
| F | 0.505 | 0.501 |

2N6157
2N6158
2N6159

PRESS FIT STUD MOUNT TRIAC



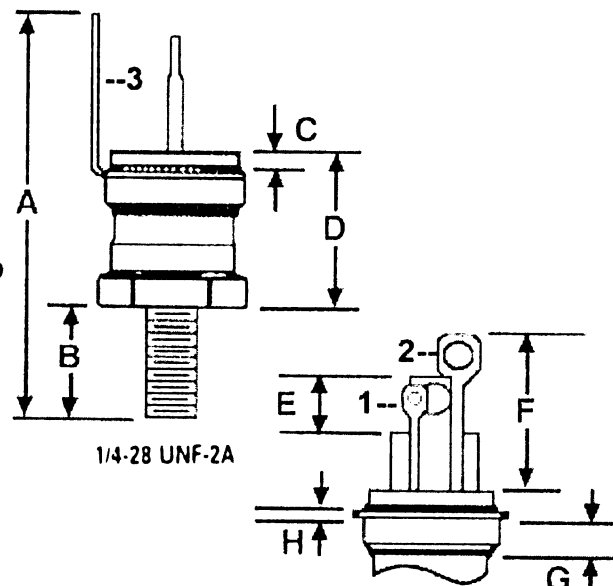
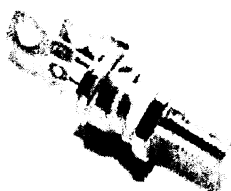
- 1. GATE
- 2. MT-1
- 3. MT-2 (stud)

| SYM. | INCHES | |
|------|--------|-------|
| A | 1.150 | |
| B | 0.114 | 0.110 |
| C | 0.453 | 0.422 |
| D | 1.603 | 1.572 |
| E | 1.243 | 1.132 |
| F | 0.562 | 0.544 |

1/4-28 UNF-2A

2N6160
2N6161
2N6162

PRESS FIT ISOLATED STUD MOUNT TRIAC



- 1. GATE
- 2. MT-1
- 3. MT-2 (collar)

| SYM. | INCHES | |
|------|--------|-------|
| A | 1.400 | |
| B | 0.453 | 0.422 |
| C | 0.090 | |
| D | 0.670 | 0.625 |
| E | 0.275 | |
| F | 0.670 | 0.610 |
| G | 0.100 | |
| H | 0.025 | |

2N6163
2N6164
2N6165

-Warning-
Isolated stud products should be handled with care. The ceramic used in these thyristers contains BERYLLIUM OXIDE as a major ingredient. DO NOT crush, grind, or abrade these portions if the thyristers because the dust resulting from such action may be HAZARDOUS if INHALED.