2N6186 thru 2N6189 (SILICON)

MEDIUM-POWER PNP SILICON TRANSISTORS

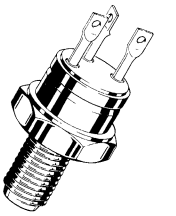
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 10 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration
- 2N6186 thru 2N6189 Complement to NPN 2N5346 thru 2N5349

10 AMPERE POWER TRANSISTORS

PNP SILICON

80-100 VOLTS
60 WATTS



*MAXIMUM RATINGS

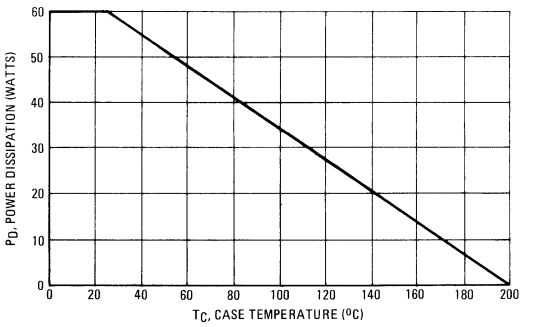
Rating	Symbol	2N6186 2N6187	2N6188 2N6189	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C	P_D	60		Watts
Derate above 25°C		343		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

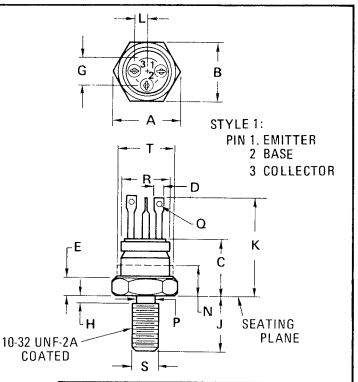
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER-TEMPERATURE DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case

CASE 160-03
(TO-59)

2N6186 thru 2N6189 (continued)

*** ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6186, 87			80	–	
	2N6188, 89			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N6186, 87			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N6188, 89			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6186, 87			–	10	
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6188, 89			–	10	
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6186, 87			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6188, 89			–	1.0	
Collector Cutoff Current		–	I_{CBO}			μAdc
(V_{CB} = Rated V_{CB}, I_E = 0)				–	10	
Emitter Cutoff Current		–	I_{EBO}			μAdc
(V_{BE} = 6 0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			30	–	
	2N6187, 89			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			30	120	
	2N6187, 89			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			20	–	
	2N6187, 89			40	–	
Collector-Emitter Saturation Voltage		9, 10, 11	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 10 Adc, I_B = 1.0 Adc)				–	1.2	
Base-Emitter Saturation Voltage		10, 11	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 10 Adc, I_B = 1.0 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)		–	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{C2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

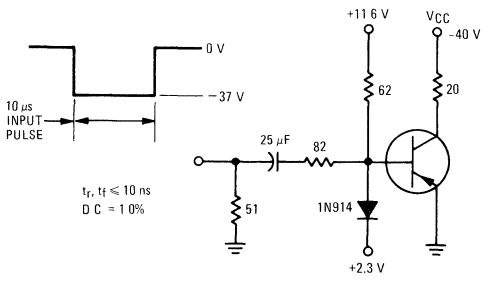


FIGURE 3 – TURN-ON TIME

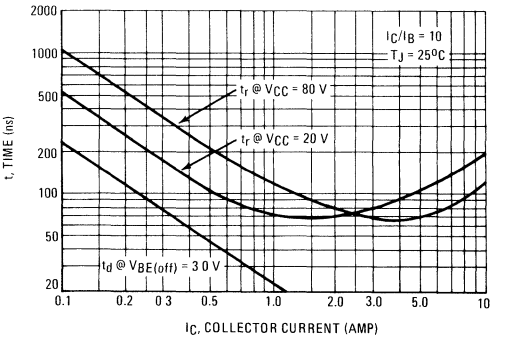


FIGURE 4 – THERMAL RESPONSE

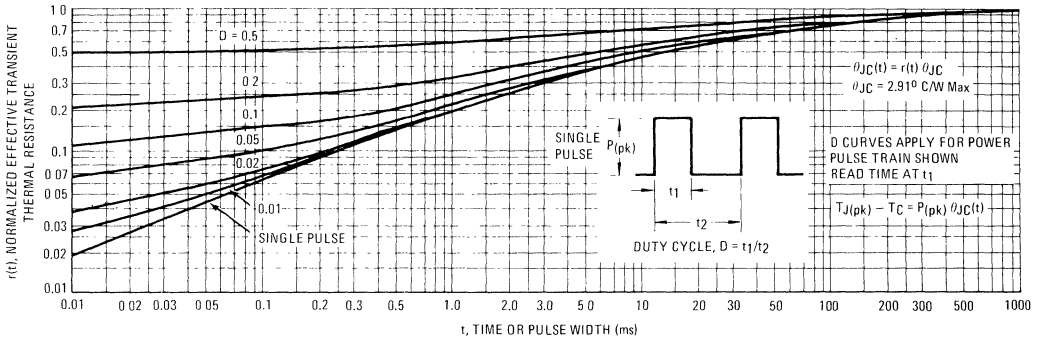
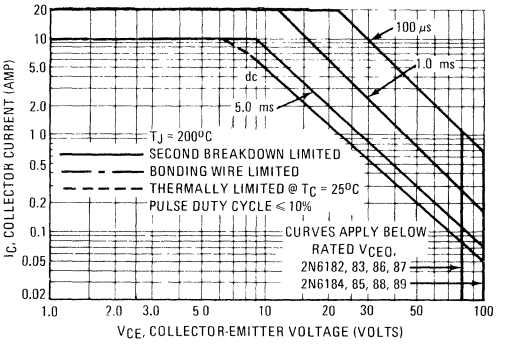


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitaitons imposed by second breakdown.

FIGURE 6 – TURN OFF TIME

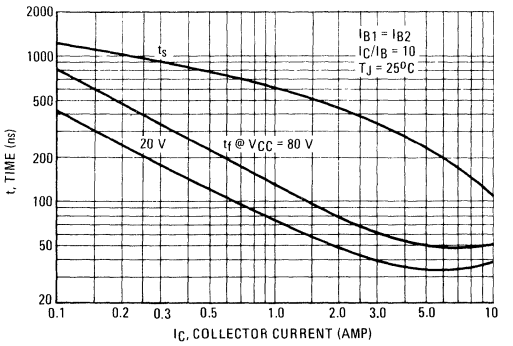


FIGURE 7 – CAPACITANCE versus VOLTAGE

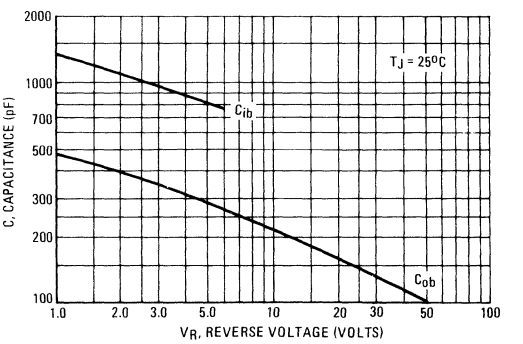


FIGURE 8 – DC CURRENT GAIN

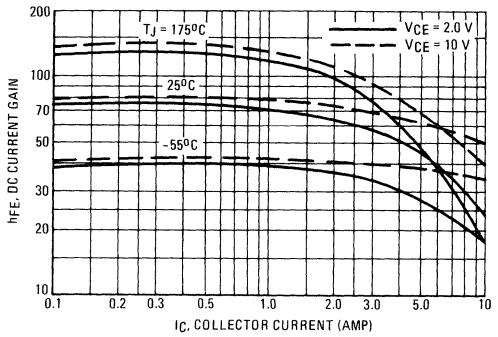


FIGURE 9 – COLLECTOR SATURATION REGION

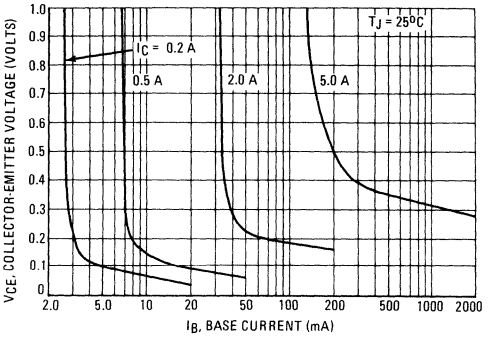


FIGURE 10 – "ON" VOLTAGES

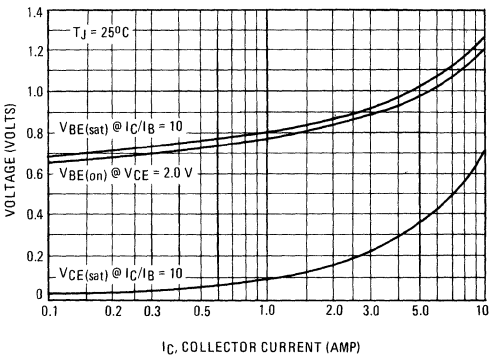


FIGURE 11 – TEMPERATURE COEFFICIENTS

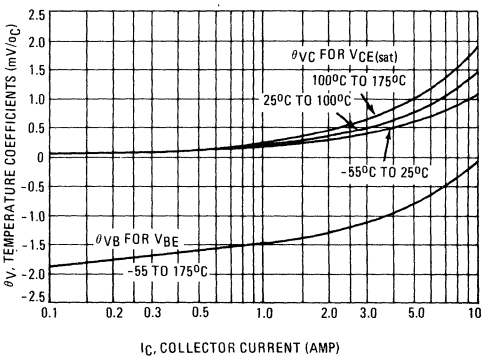


FIGURE 12 – COLLECTOR CUT-OFF REGION

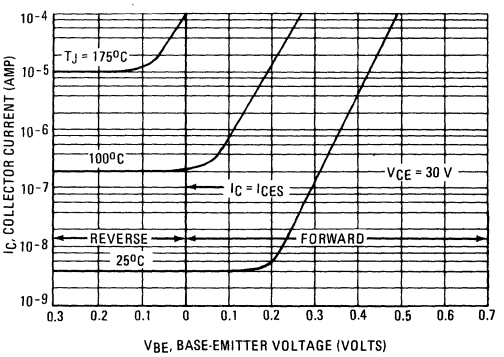


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE