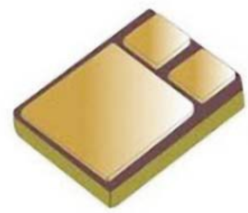
2N6193U3

PNP Switching Silicon Transistor

Rev. V5

Features

- JAN, JANTX, JANTXV, JANS and JANSR Qualified to MIL-PRF-19500/561
- JEDEC Registered 2N6193
- Lightweight & Low Power
- Ideal for Space, Military, and Other High Reliability Applications
- Surface Mount U3 (TO-276AA) Package



Electrical Characteristics (T_A = +25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	I_C = -50 mA dc	$V_{(BR)CEO}$	V dc	-100	—
Collector - Emitter Cutoff Current	V_{CE} = -100 V dc	I_{CEO}	µA dc	—	-100
Collector - Emitter Cutoff Current	V_{BE} = +1.5 Vdc; V_{CE} = -90 V dc	I_{CEX1}	µA dc	—	-10
Collector - Base Cutoff Current	V_{CB} = -100 V dc	I_{CBO}	µA dc	—	-10
Emitter - Base Cutoff Current	V_{EB} = -6.0 V dc	I_{EBO}	µA dc	—	-100
Forward - Current Transfer Ratio	V_{CE} = -2.0 V dc; I_C = -0.5 A dc V_{CE} = -2.0 V dc; I_C = -2.0 A dc V_{CE} = -2.0 V dc; I_C = -5.0 A dc	h_{FE}	-	60 60 40	240
Collector - Emitter Saturation Voltage	I_C = -2.0 A dc; I_B = -0.2 A dc I_C = -5.0 A dc; I_B = -0.5 A dc	$V_{CE(SAT)1}$ $V_{CE(SAT)2}$	V dc	—	-0.7 -1.2
Emitter - Base Saturation Voltage	I_C = -2.0 A dc; I_B = -0.2 A dc I_C = -5.0 A dc; I_B = -0.5 A dc	$V_{BE(SAT)1}$ $V_{BE(SAT)2}$	V dc	—	-1.2 -1.8
Collector - Emitter Cutoff Current	T_A = +150°C V_{CE} = -90 V dc; V_{BE} = +1.5 Vdc	I_{CEX2}	µA dc	—	-15
Forward - Current Transfer Ratio	T_A = -55°C V_{CE} = -2.0 V dc; I_C = -2.0 A dc	h_{FE4}	-	12	
Dynamic Characteristics					
Small-Signal Short-Circuit Forward - Current Transfer Ratio	V_{CE} = -10.0 V dc; I_C = -0.5 A dc; f = 10 MHz	$\mid h_{fe} \mid$	-	3	15
Output Capacitance	V_{CB} = -10 V dc, I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}	pF	—	300
Input Capacitance	V_{BE} = -2 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}	pF	—	1250
Switching Characteristics					
Delay Time	See figure 11 of MIL-PRF-19500/561	t_d	ns	—	100
Rise Time	See figure 11 of MIL-PRF-19500/561	t_r	ns	—	100
Storage Time	See figure 12 of MIL-PRF-19500/561	t_s	µs	—	2.0
Fall Time	See figure 12 of MIL-PRF-19500/561	t_f	ns	—	200

For further information and support please visit:
info@vptcomponents.com

Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)

Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	-100 V dc
Collector - Base Voltage	V_{CBO}	-100 V dc
Emitter - Base Voltage	V_{EBO}	-6.0 V dc
Base Current	I_B	-1.0 A dc
Collector Current	I_C	-5.0 A dc
Total Power Dissipation @ T_A = +25°C (1) @ T_C = +25°C (2)	P_T	 1.0 W 100 W
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to +200°C

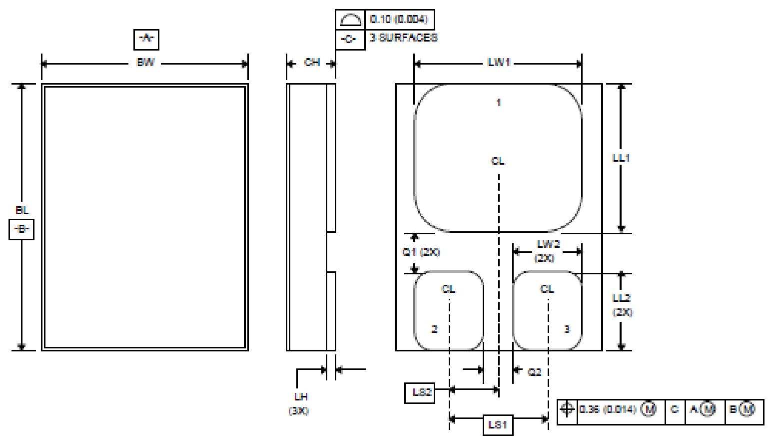
(1) See figure 6 of MIL-PRF-19500/561
(2) See figure 7 and 8 of MIL-PRF-19500/561

Thermal Characteristics

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	175°C/W

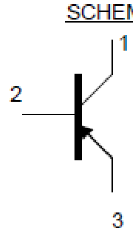
Safe Operating Area	
DC Tests:	T_C = +25°C; t ≥ 0.5 s; I Cycle
Test 1:	V_{CE} = -2.0 V dc; I_C = -5.0 A dc
Test 2:	V_{CE} = -90 V dc; I_C = -55 mA dc

Outline Drawing (U3)



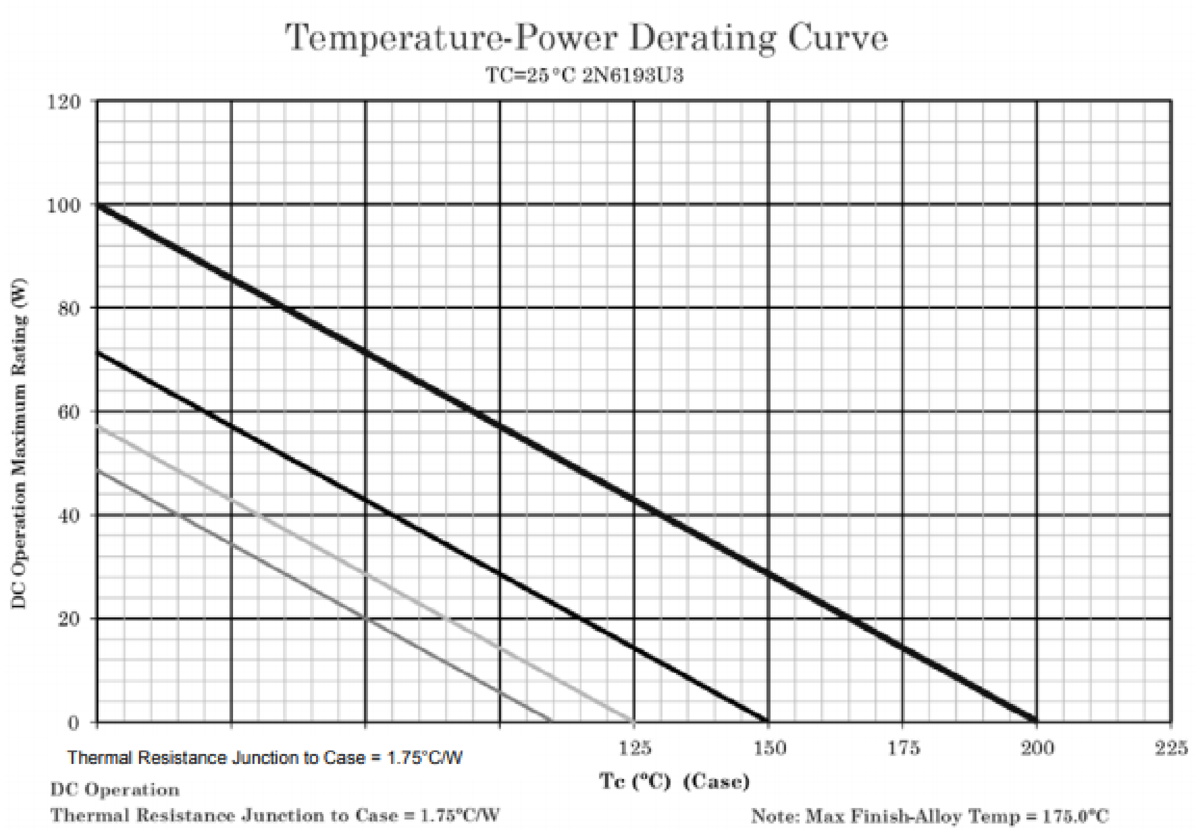
Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH	.1085	.1205	2.76	3.06
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	

SCHEMATIC



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
4. Terminal 1 - collector, terminal 2 -base, terminal 3 - emitter.

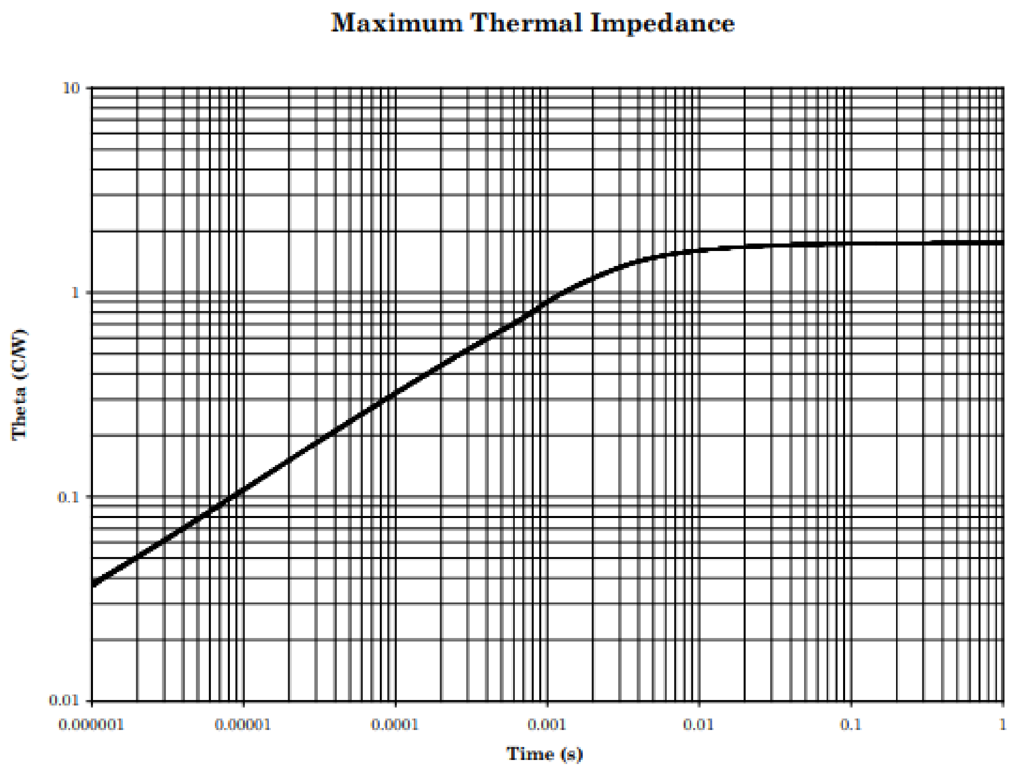
FIGURE 5. Physical dimensions and configuration 2N6193U3.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 8. Temperature-power derating for 2N6193U3 $R_{\theta JC}$ (U3 package).



Solder mounted to copper heatsink at T_C = +25°C thermal resistance = 1.75°C/W, Pdiss = 100W.

FIGURE 10. Thermal impedance graph ($R_{\theta JC}$) for 2N6193U3 (U3).

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