2N6256

CASE 249-05, STYLE 1 UHF AMPLIFIER TRANSISTOR



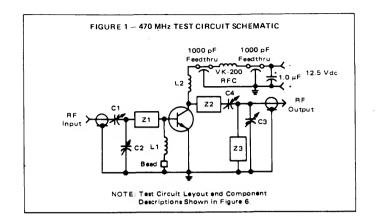
NPN SILICON

MAXIMUM RATINGS

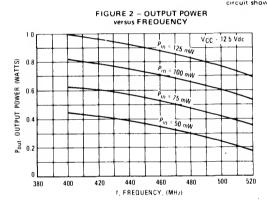
Rating	Symbol	Value	Unit Vdc			
Collector-Emitter Voltage	VCEO	16				
Collector-Base Voltage	VCBO	36	Vdc			
Emitter-Base Voltage	VEBO	4.0	Vdc			
Collector Current — Continuous	lc	0.4	Adc			
Total Device Dissipation @ T _C = 25°C Derate above 25°C	PD	2.0 11.4	Watts mW/°C			
Storage Temperature	T _{stg}	-65 to +200	°C			

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted.)

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I _C = 5.0 mAdc, I _B = 0)		V(BR)CEO	16	_		Vdc
Collector-Emitter Breakdown Voltage (I _C = 5.0 mAdc, V _{BE} = 0)		V(BR)CES	36			Vdc
Emitter-Base Breakdown Voltage (I _E = 1.0 mAdc, I _C = 0)		V(BR)EBO	4.0		_	Vdc
Collector Cutoff Current (V _{CB} = 15 Vdc, I _E = 0)		ІСВО	-	_	0.5	mAdc
Collector Cutoff Current (VCE = 15 Vdc, VBE = 0, T _A = 125°C)		ICES		_	5.0	mAdc
ON CHARACTERISTICS						
DC Current Gain (I _C = 50 mAdc, V _{CE} = 5.0 Vdc)		hFE	20	80	200	_
SMALL SIGNAL CHARACTERISTICS						
Output Capacitance (VCB = 12.5 Vdc, I _E = 0, f = 1.0 MHz)		C _{obo}	_	6.0	8.0	pF
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain (Pout = 0.5 W, V _{CC} = 12.5 Vdc, f = 470 MHz)	(Figures 1, 6)	GPE	7.0	9.0	_	dB
Collector Efficiency (P _{out} = 0.5 W, V _{CC} = 12.5 Vdc, f = 470 MHz)	(Figures 1, 6)	η	60	70	_	%



Typical Output Power curves were measured in circuit shown in Figure 6



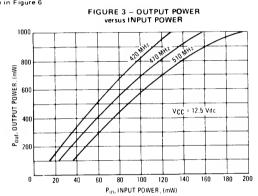
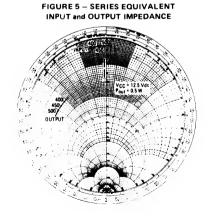
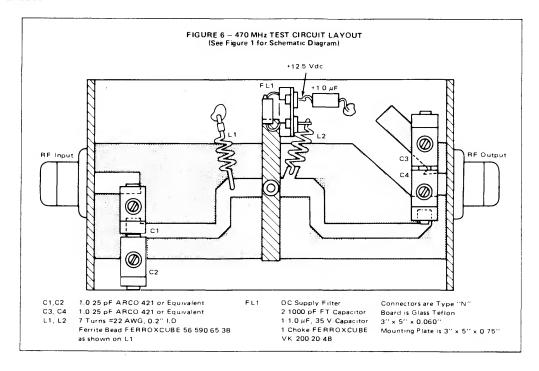
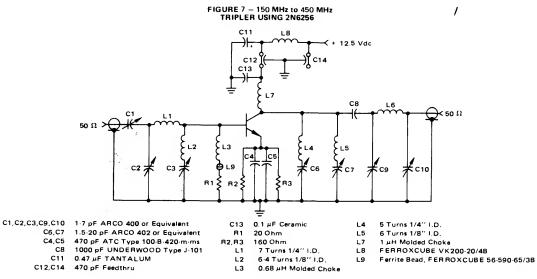


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE 1000 800 Pout, OUTPUT POWER (mW) f = 470 MHz 100 mW 600 400 = 50 mW 200 Pin = 25 mW 7.0 9.0 10 5.0 VCC. SUPPLY VOLTAGE (VOLTS)







NOTE: All coils air core spece wound with #20 AWG Wire, unless otherwise specified.

Figure 7 shows the 2N6256 in a 150 MHz to 450 MHz tripler circuit. This circuit will typically produce 85 mW at 450 MHz with 30 mW at 150 MHz input (4.5 dB gain). Collector efficiency is 25% and all unwanted harmonics are at least 30 dB down from the 450 MHz output level.

It is important that each emitter lead be bypassed separately with a good hi-quality capacitor. The emitter resistor is likewise split in two with one-half on each emitter lead.

The input network is a modified "TEE" consisting of C1, C2, and L1, which matches the 50 Ohm input to the transistor impedance at 150 mc; this is roughly 18-j20 Ohms. The combination of L2 and C3 form a 450 MHz idler to provide a base return for third harmonic current. L4, C6 and L5, C7 are 150 MHz and 300 MHz output idlers respectively. The output matching section is a pi network made up of L6, C9 and C10. All coils are air core space-wound (turns one wire diameter apart) with #20 AWG wire.