

High-Power NPN Silicon Transistors

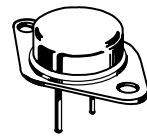
... designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining —
 $V_{CEO(sus)} = 100 \text{ Vdc (Min)} \text{ — } 2\text{N}6274$
 $= 120 \text{ Vdc (Min)} \text{ — } 2\text{N}6275$
 $= 150 \text{ Vdc (Min)} \text{ — } 2\text{N}6277$
- High DC Current Gain —
 $h_{FE} = 30\text{--}120 \text{ @ } I_C = 20 \text{ Adc}$
 $= 10 \text{ (Min) @ } I_C = 50 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 20 \text{ Adc}$
- Fast Switching Times @ $I_C 20 \text{ Adc}$
 $t_r = 0.35 \text{ ms (Max)}$
 $t_s = 0.8 \text{ ms (Max)}$
 $t_f = 0.25 \text{ ms (Max)}$
- Complement to 2N6377–79

2N6274
2N6275
2N6277*

*ON Semiconductor Preferred Device

50 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
250 WATTS



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS(1)

Rating	Symbol	2N6274	2N6275	2N6277	Unit
Collector–Base Voltage	V_{CB}	120	140	180	Vdc
Collector–Emitter Voltage	V_{CEO}	100	120	150	Vdc
Emitter–Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak	I_C	50 100			A dc
Base Current	I_B	20			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

2N6274 2N6275 2N6277

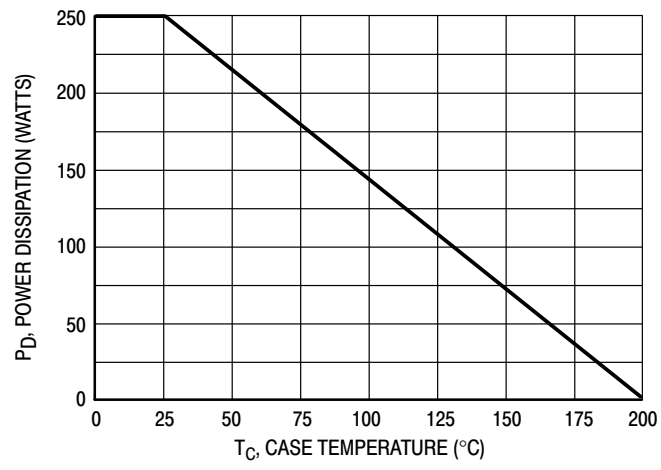


Figure 1. Power Derating

2N6274 2N6275 2N6277

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) $I_C = 50 \text{ mAdc}, I_B = 0$	2N6274 2N6275 2N6277	$V_{CEO(sus)}$	100 120 150	— — —	Vdc
Collector Cutoff Current ($V_{CE} = 50 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$) ($V_{CE} = 75 \text{ Vdc}, I_B = 0$)	2N6274 2N6275 2N6277	I_{CEO}	— — —	50 50 50	μAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}, V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)		I_{CEX}	— —	10 1.0	μAdc mAdc
Emitter Cutoff Current ($V_{BE} = 6.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	100	μAdc

ON CHARACTERISTICS (1)

DC Current Gain $I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$ $I_C = 20 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$ $I_C = 50 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$		h_{FE}	50 30 10	— 120 —	—
Collector–Emitter Saturation Voltage $I_C = 20 \text{ Adc}, I_B = 2.0 \text{ Adc}$ $I_C = 50 \text{ Adc}, I_B = 10 \text{ Adc}$		$V_{CE(sat)}$	— —	1.0 3.0	Vdc
Base–Emitter Saturation Voltage $I_C = 20 \text{ Adc}, I_B = 2.0 \text{ Adc}$ $I_C = 50 \text{ Adc}, I_B = 10 \text{ Adc}$		$V_{BE(sat)}$	— —	1.8 3.5	Vdc
Base–Emitter On Voltage ($I_C = 20 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)		$V_{BE(on)}$	—	1.8	Vdc

DYNAMIC CHARACTERISTICS

Current–Gain Bandwidth Product (2) ($I_C = 1.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f_{test} = 10 \text{ MHz}$)		f_T	30	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)		C_{ob}	—	600	pF

SWITCHING CHARACTERISTICS

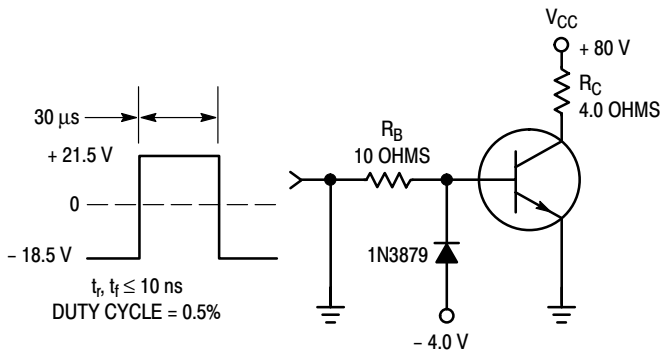
Rise Time ($V_{CC} = 80 \text{ Vdc}, I_C = 20 \text{ Adc}, I_{B1} = 2.0 \text{ Adc}, V_{BE(off)} = 5.0 \text{ Vdc}$)		t_r	—	0.35	μs
Storage Time ($V_{CC} = 80 \text{ Vdc}, I_C = 20 \text{ Adc}, I_{B1} = I_{B2} = 2.0 \text{ Adc}$)		t_s	—	0.80	μs
Fall Time ($V_{CC} = 80 \text{ Vdc}, I_C = 20 \text{ Adc}, I_{B1} = I_{B2} = 2.0 \text{ Adc}$)		t_f	—	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$

2N6274 2N6275 2N6277



NOTE: For information of Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

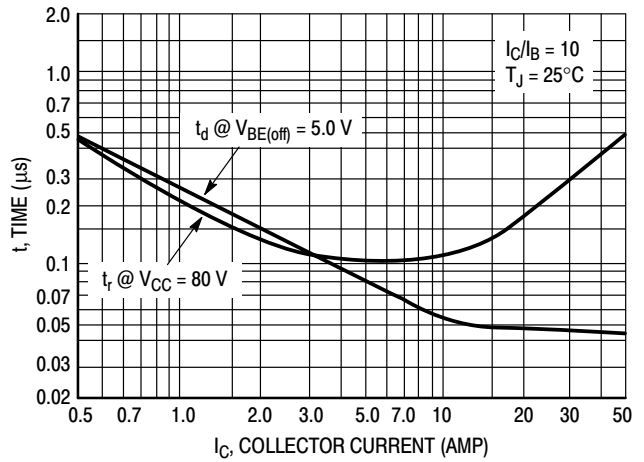


Figure 3. Turn-On Time

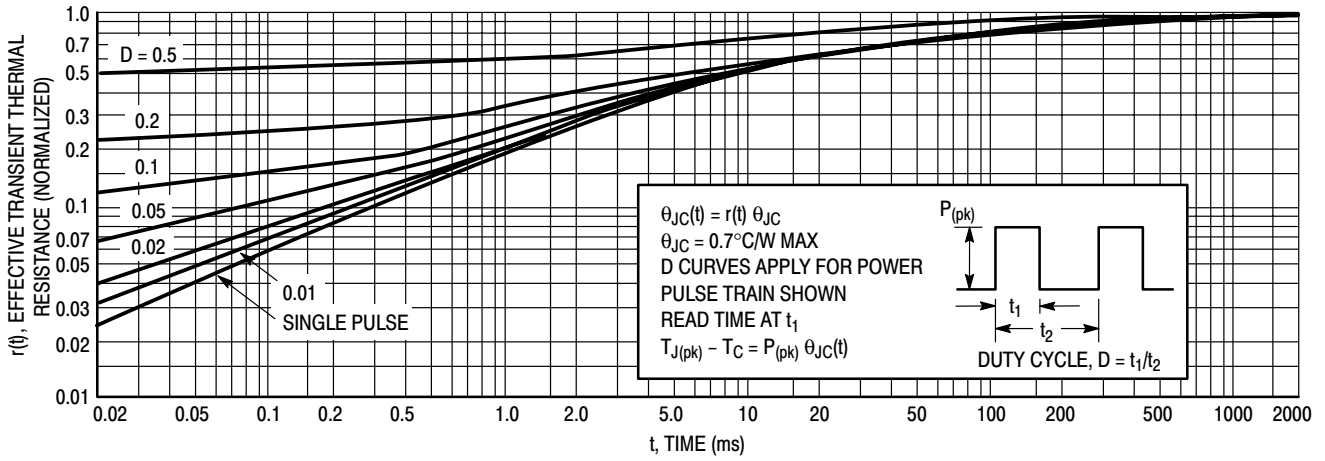


Figure 4. Thermal Response

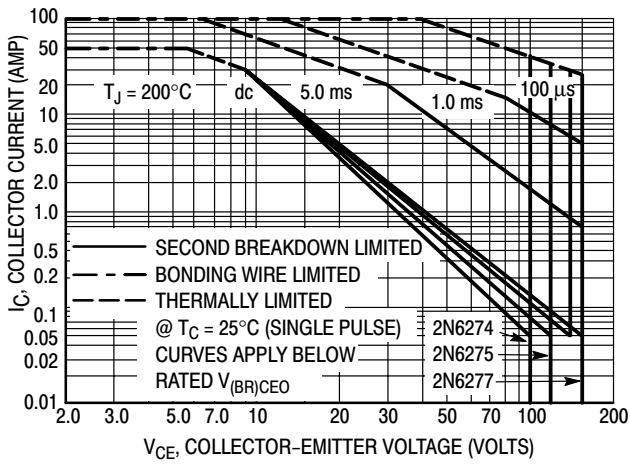


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

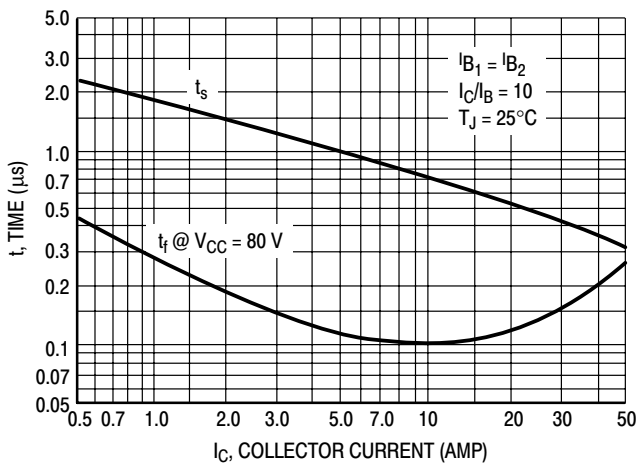


Figure 6. Turn-Off Time

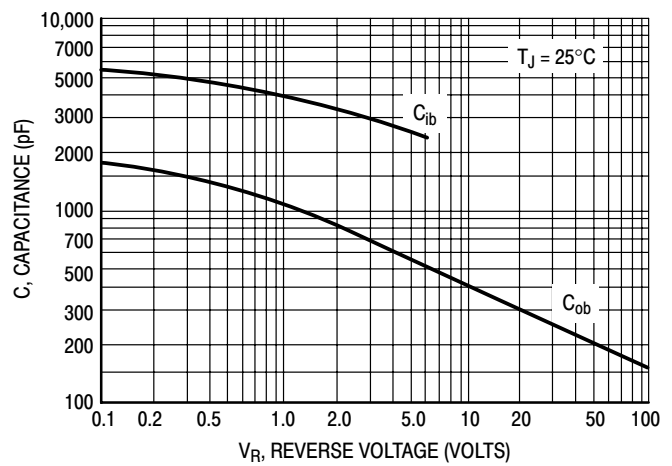


Figure 7. Capacitance

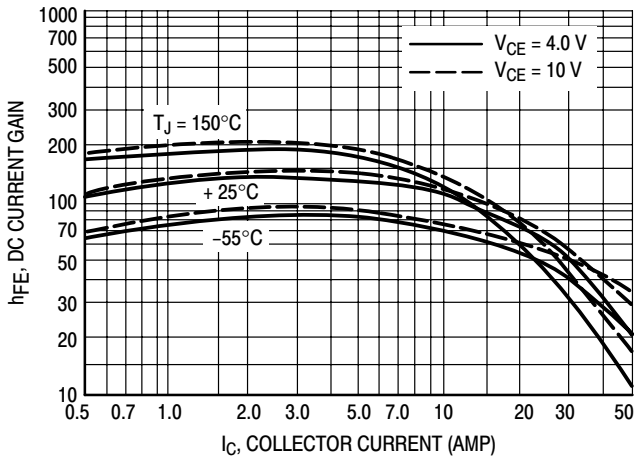


Figure 8. DC Current Gain

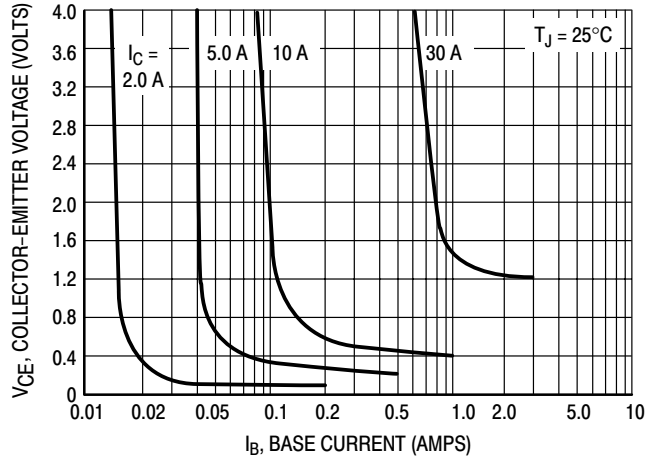


Figure 9. Collector Saturation Region

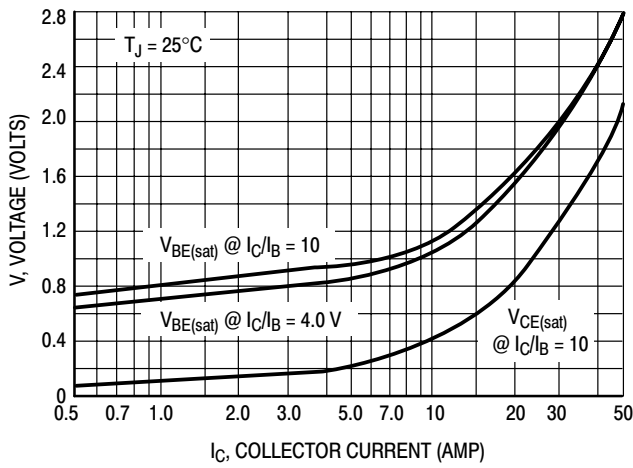


Figure 10. "On" Voltages

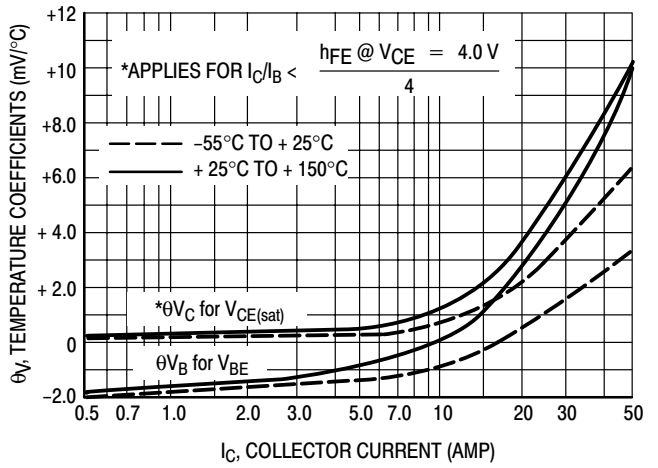


Figure 11. Temperature Coefficients

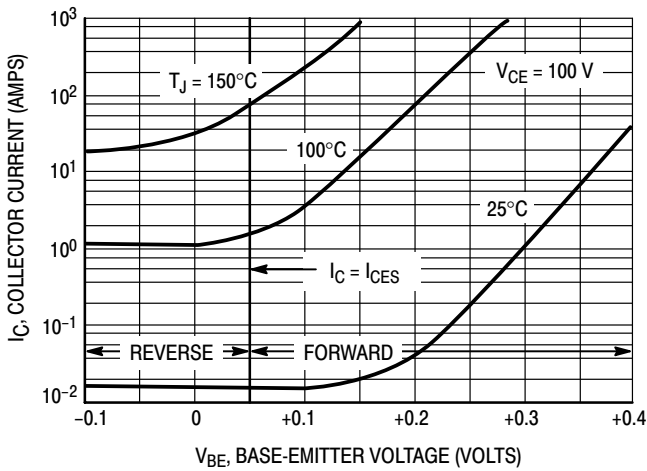


Figure 12. Collector Cut-off Region

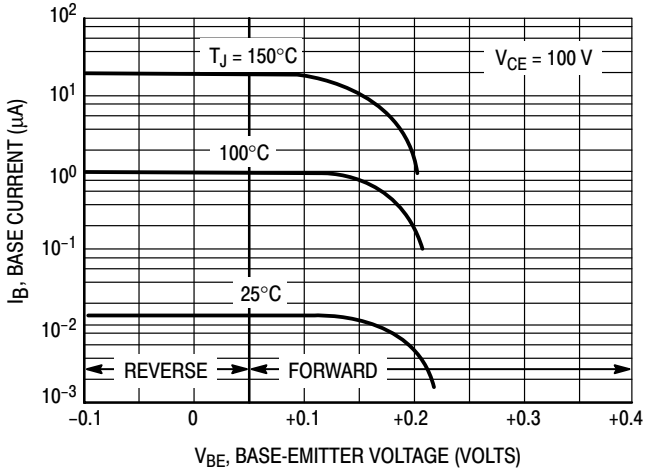
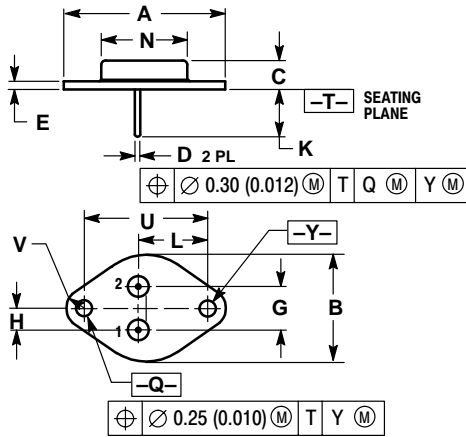


Figure 13. Base Cut-off Region

2N6274 2N6275 2N6277

PACKAGE DIMENSIONS


CASE 197A-05 TO-204AE ISSUE J



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

- STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

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