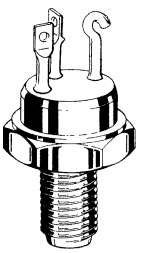
2N6278 thru 2N6281 (SILICON)

HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6278
  = 120 Vdc (Min) – 2N6279
  = 140 Vdc (Min) – 2N6280
  = 150 Vdc (Min) – 2N6281
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)

50 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
250 WATTS



*MAXIMUM RATINGS

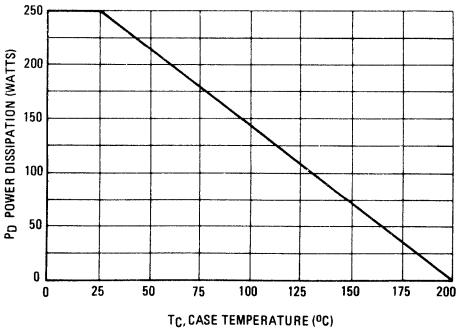
Rating	Symbol	2N6278	2N6279	2N6280	2N6281	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current – Continuous Peak	I_C	50 100				Adc
Base Current	I_B	20				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43				Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200				°C

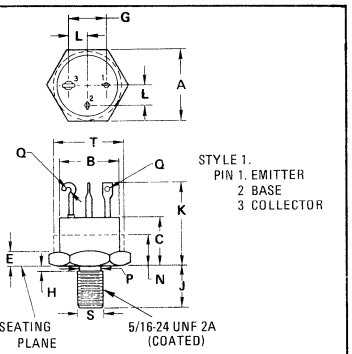
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.70	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.72	22.23	0.855	0.875
B	18.92	19.69	0.745	0.775
C	12.19	13.59	0.480	0.535
E	2.29	4.24	0.090	0.167
G	12.32	13.08	0.485	0.515
H	–	2.67	–	0.105
J	11.68	12.57	0.460	0.495
K	23.80	26.16	0.937	1.030
L	6.10	6.60	0.240	0.260
N	–	7.62	–	0.300
P	7.06	7.92	0.278	0.312
Q	1.52	2.67	0.060	0.105
S	7.127	7.249	0.2806	0.2854
T	19.69	22.23	0.775	0.875

All JEDEC notes and dimensions apply.
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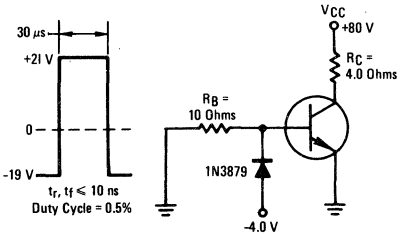
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6278	$V_{CEO(sus)}$	100	–	Vdc
	2N6279		120	–	
	2N6280		140	–	
	2N6281		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6278		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6279		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6280		–	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6281		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			–	10	μAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C			–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)			30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–		Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.2	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.5	
Base-Emitter On Voltage (I_C = 20 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	600	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = 2.0 Adc, $V_{BE\ (off)}$ = 5.0 Vdc)		t_r	–	0.35	μs
Storage Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_s	–	0.80	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data (1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



Note: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN ON TIME

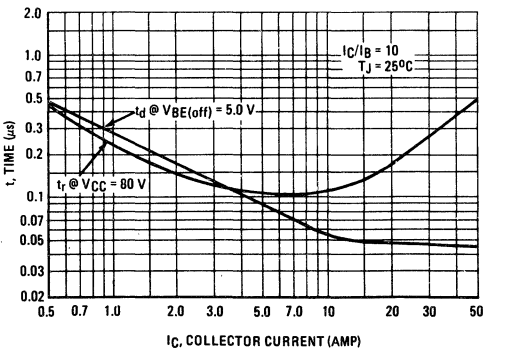


FIGURE 4 – THERMAL RESPONSE

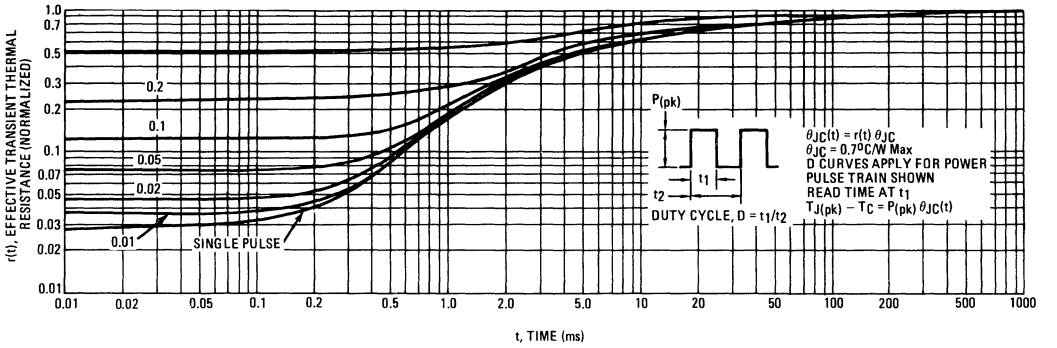
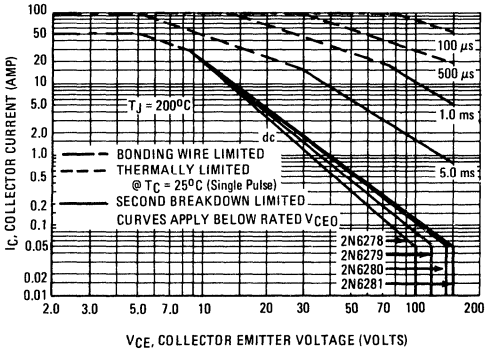


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN OFF TIME

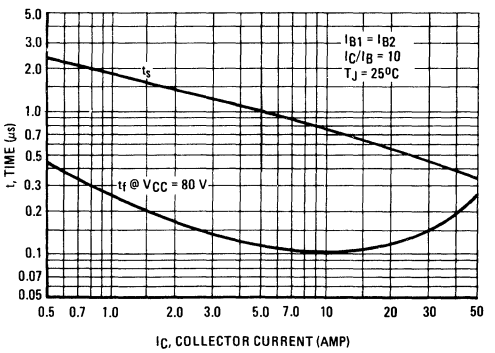


FIGURE 7 – CAPACITANCE

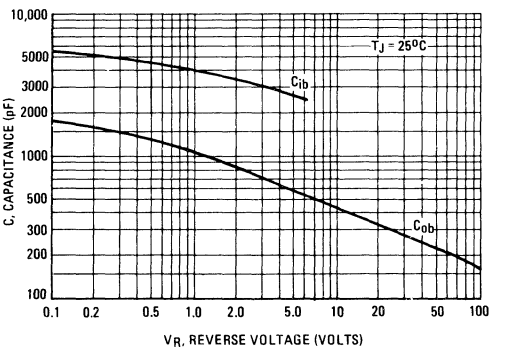


FIGURE 8 – DC CURRENT GAIN

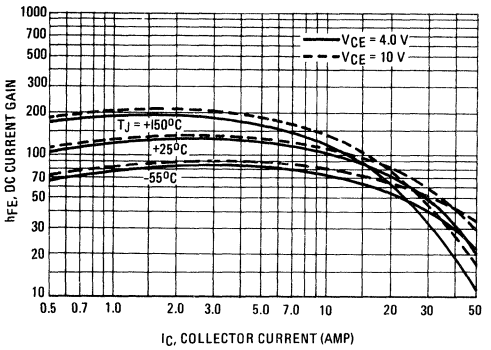


FIGURE 9 – COLLECTOR SATURATION REGION

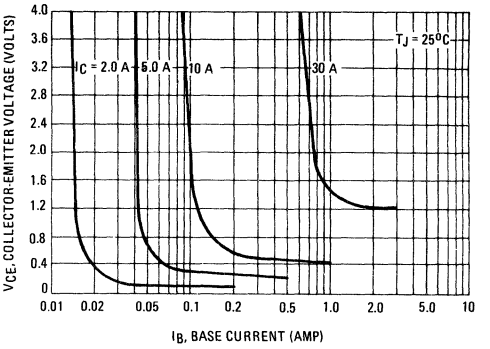


FIGURE 10 – ON VOLTAGES

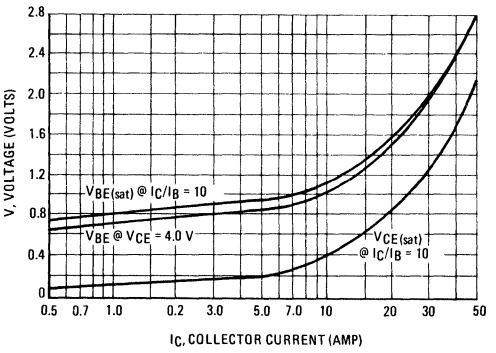


FIGURE 11 – TEMPERATURE COEFFICIENTS

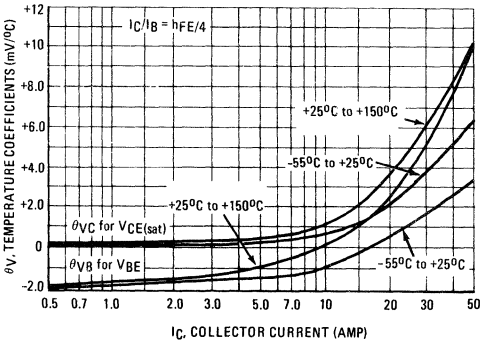


FIGURE 12 – COLLECTOR CUTOFF REGION

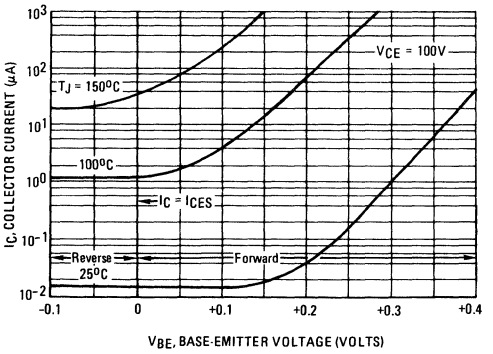


FIGURE 13 – BASE CUTOFF REGION