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High-Power NPN Silicon Transistors

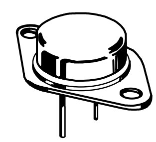
2N6338
2N6339
2N6340
2N6341*

*Motorola Preferred Device

. . . designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N6338
  = 120 Vdc (Min) — 2N6339
  = 140 Vdc (Min) — 2N6340
  = 150 Vdc (Min) — 2N6341
- High DC Current Gain —
  h_{FE} = 30 – 120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 µs (Max)
  t_s = 1.0 µs (Max)
  t_f = 0.25 µs (Max)
- Complement to 2N6436–38

25 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector–Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector–Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter–Base Voltage	V_{EB}	6.0				Vdc
Collector Current Continuous Peak	I_C	 25 50				Adc
Base Current	I_B	10				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 200 1.14				 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

* Indicates JEDEC Registered Data.

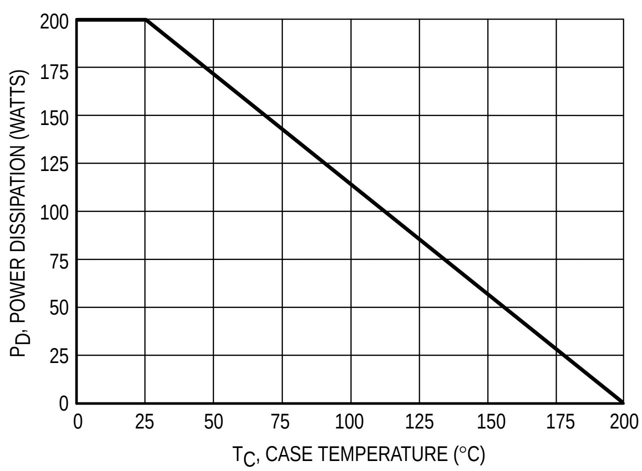


Figure 1. Power Derating

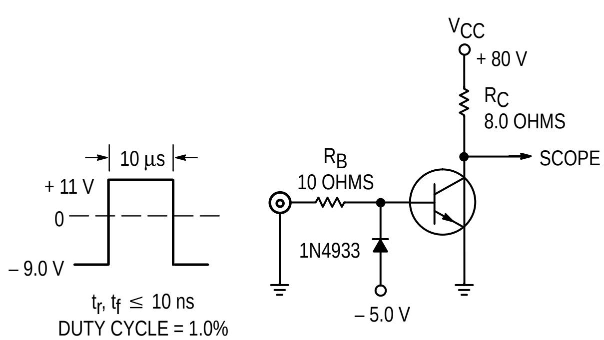
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6338 2N6339 2N6340 2N6341	$V_{CEO(sus)}$	100 120 140 150	— — — —	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0) (V_{CE} = 75 Vdc, I_B = 0)	 2N6338 2N6339 2N6340 2N6341	I_{CEO}	 — — — —	 50 50 50 50	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 — —	 10 1.0	 μAdc mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain) (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 50 30 12	 — 120 —	—
Collector Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{CE(sat)}$	 — —	 1.0 1.8	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	 — —	 1.8 2.5	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	300	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)		t_r	—	0.3	μs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	—	1.0	μs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	—	0.25	μs

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.



NOTE: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

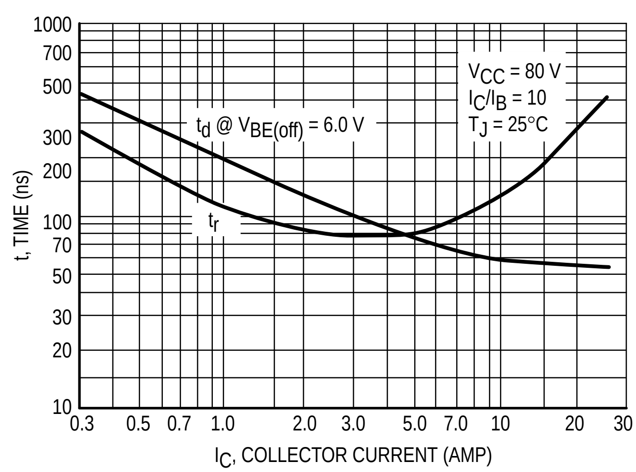


Figure 3. Turn–On Time

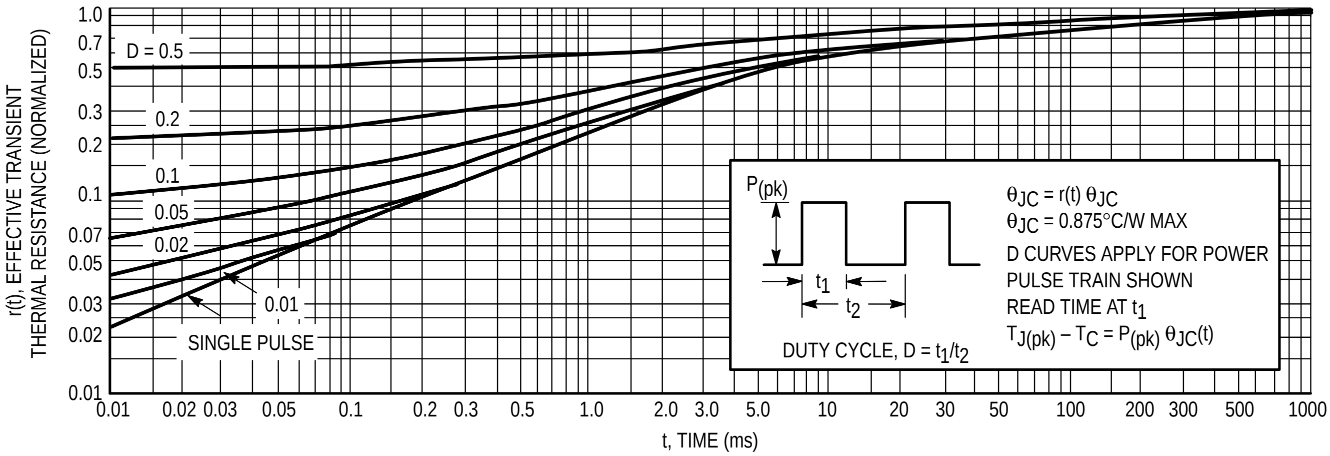


Figure 4. Thermal Response

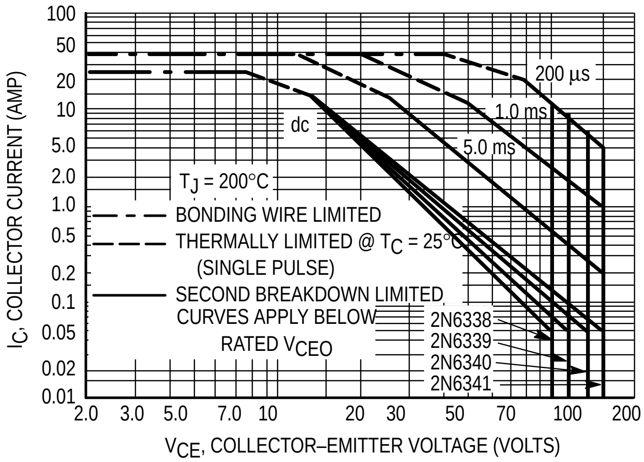


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

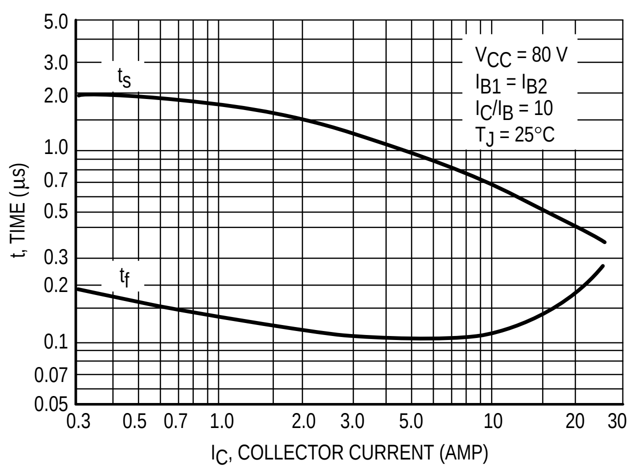


Figure 6. Turn–Off Time

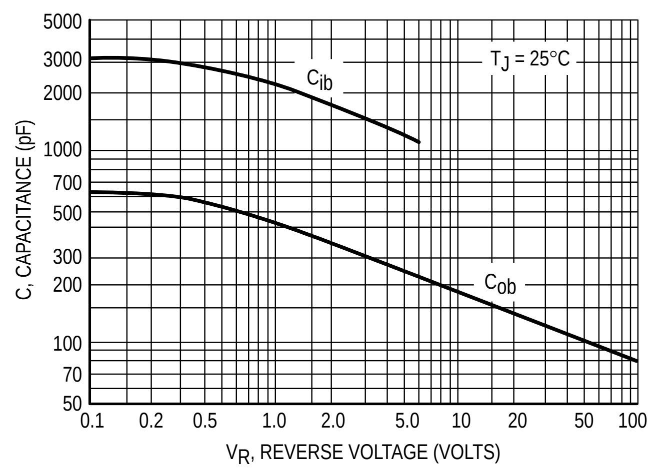
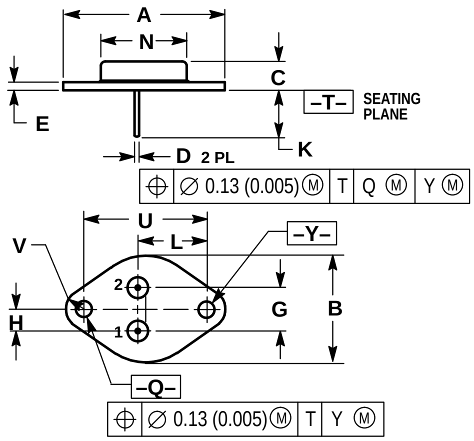


Figure 7. Capacitance

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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