2N6412, 2N6413 NPN (SILICON)

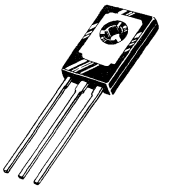
2N6414, 2N6415 PNP

COMPLEMENTARY PLASTIC SILICON ANNULAR POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high-speed switching applications.

- Low Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N6412, 2N6414
  = 60 Vdc (Min) – 2N6413, 2N6415
- High Current-Gain – Bandwidth Product –
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- DC Current Gain Specified at 0.2, 1.0, 2.0 and 4.0 Adc
- Collector-Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc
- Pin Compatible With TO-220AB Package

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40, 60 VOLTS
15 WATTS



*MAXIMUM RATINGS

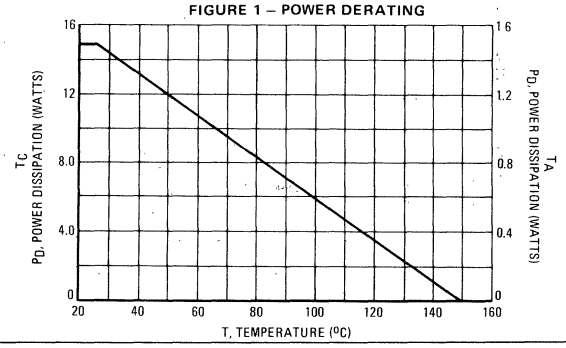
Rating	Symbol	2N6412 2N6414	2N6413 2N6415	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0		Adc Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

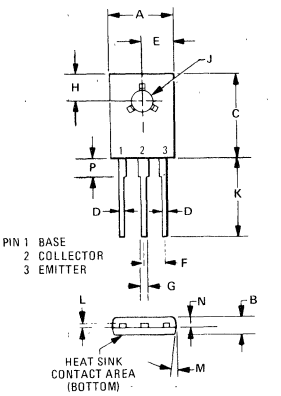
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.295	0.305	7.490	7.750
B	0.095	0.105	2.410	2.670
C	0.425	0.435	10.800	11.050
D	0.020	0.026	0.508	0.660
E	0.145	0.155	3.680	3.940
F	0.093 TP		2.360 TP	
G	0.025	0.035	0.635	0.889
H	0.148	0.158	3.760	4.010
J	0.115	0.118	2.920	3.000
K	0.595	0.645	15.110	16.380
L	0.015	0.025	0.381	0.635
M	30° TYP		30° TYP	
N	0.045	0.055	1.140	1.400
P	0.085	0.095	2.160	2.410

CASE 77-03

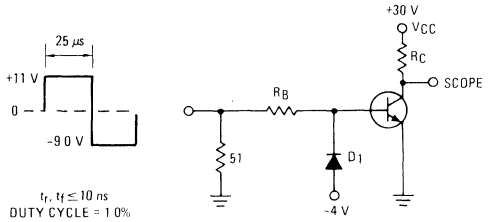
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	2N6412, 2N6414		40	–	
	2N6413, 2N6415		60	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6412, 2N6414		–	100	
(V_{CE} = 30 Vdc, I_B = 0)	2N6413, 2N6415		–	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6412, 2N6414		–	1.0	μAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6413, 2N6415		–	1.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6412, 2N6414		–	0.1	mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C	2N6413, 2N6415		–	0 1	
Emitter Cutoff Current		I_{EBO}	–	1.0	μAdc
(V_{EB} = 6.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			25	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.4	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	0.6	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	0.8	
(I_C = 4.0 Adc, I_B = 800 mAdc)			–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	1 8	Vdc
(I_C = 2.0 Adc, I_B = 200 mAdc)					
Base-Emitter on Voltage		$V_{BE(on)}$	–	1.8	Vdc
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	50	–	MHz
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0)	2N6412, 2N6413		–	50	
f = 0.1 MHz)	2N6414, 2N6415		–	70	
Small-Signal Current Gain		h_{fe}	10	–	–
(I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ~100 mA
MSD6100 USED BELOW I_B ~100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

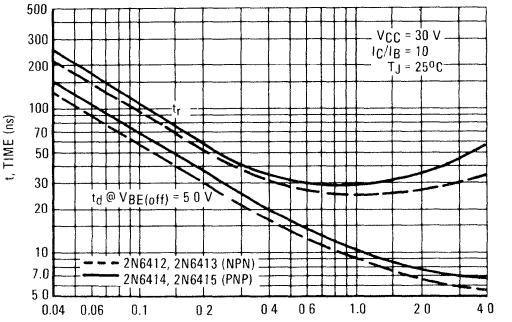


FIGURE 4 – THERMAL RESPONSE

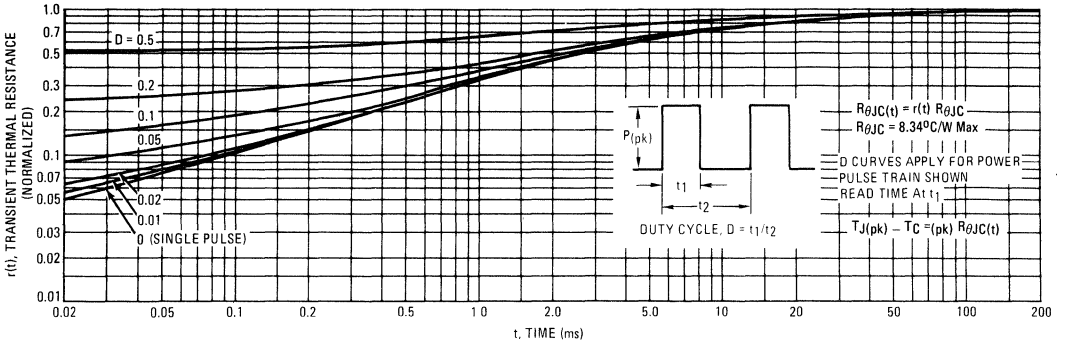
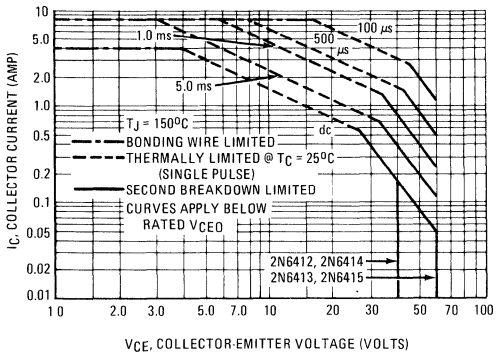


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i e , the transistor must not be subjected to greater dissipation than the curves indicate

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4 At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (See AN-415A)

FIGURE 6 – TURN-OFF TIME

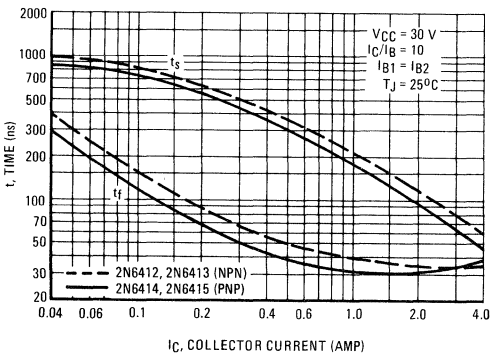
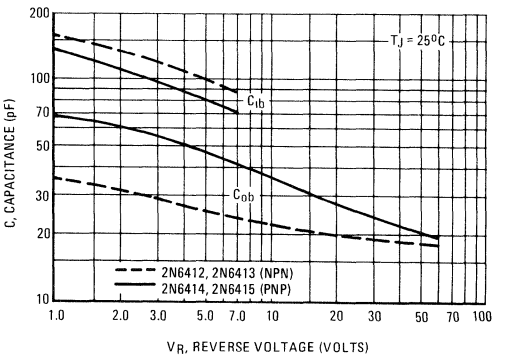


FIGURE 7 – CAPACITANCE



NPN
2N6412, 2N6413

PNP
2N6414, 2N6415

FIGURE 8 – DC CURRENT GAIN

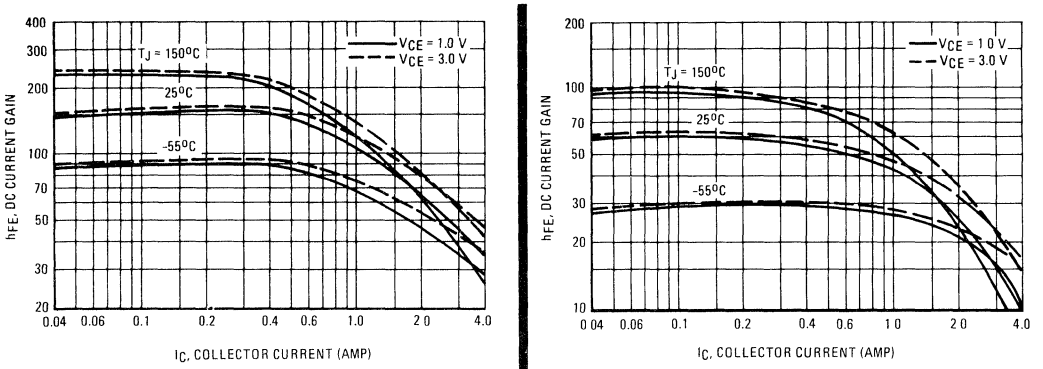


FIGURE 9 – "ON" VOLTAGES

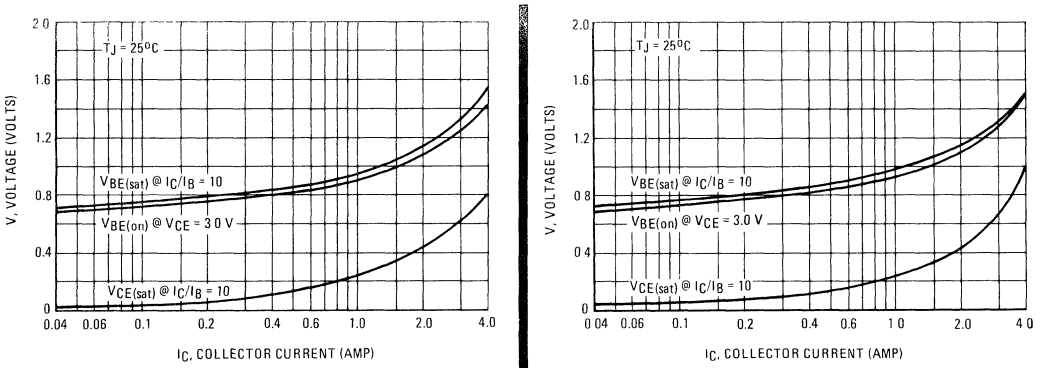


FIGURE 10 – TEMPERATURE COEFFICIENTS