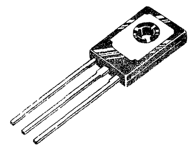
2N6416, 2N6417 NPN (SILICON)
2N6418, 2N6419 PNP

COMPLEMENTARY PLASTIC SILICON ANNULAR POWER TRANSISTORS

. . . designed for low power audio amplifier and low-current, high speed switching applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6416, 2N6418
  = 100 Vdc (Min) — 2N6417, 2N6419
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40-250
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain — Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc)
- Pin Compatible With TO-220AB Package

3 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS



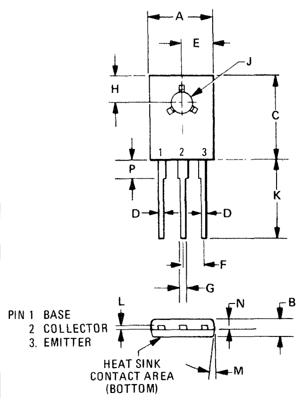
*MAXIMUM RATINGS

Rating	Symbol	2N6416 2N6418	2N6417 2N6419	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	3.0 6.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

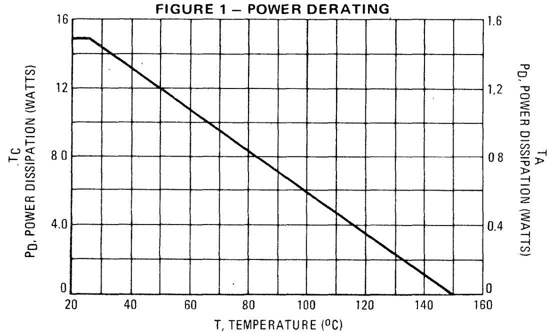
*Indicates JEDEC Registered Data.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0 295	0.305	7.490	7 750
B	0.095	0.105	2.410	2.670
C	0.425	0.435	10.800	11.050
D	0.020	0.026	0 508	0.660
E	0.145	0.155	3.680	3 940
F	0 093 TP		2.360 TP	
G	0 025	0.035	0 635	0.889
H	0.148	0.158	3 760	4.010
J	0.115	0.118	2.920	3.000
K	0.595	0.645	15.110	16.380
L	0.015	0 025	0.381	0.635
M	3° TYP		3° TYP	
N	0.045	0.055	1.140	1.400
P	0.085	0 095	2 160	2.410

CASE 77-03

FIGURE 1 — POWER DERATING

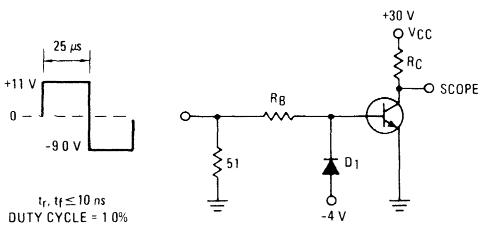


***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	2N6416, 2N6418		80	–	
	2N6417, 2N6419		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6416, 2N6418		–	100	
(V_{CE} = 50 Vdc, I_B = 0)	2N6417, 2N6419		–	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6416, 2N6418		–	1.0	μAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6417, 2N6419		–	1.0	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6416, 2N6418		–	0.1	mAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6417, 2N6419		–	0.1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			10	–	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	2.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 200 mAdc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	40	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0, f = 0.1 MHz	2N6416,2N6417		–	50	
	2N6418,2N6419		–	70	
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	–	–

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 — TURN-ON TIME

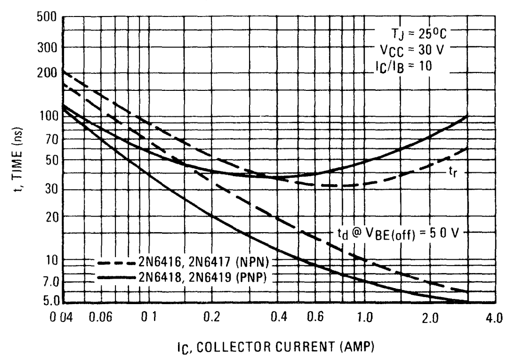


FIGURE 4 – THERMAL RESPONSE

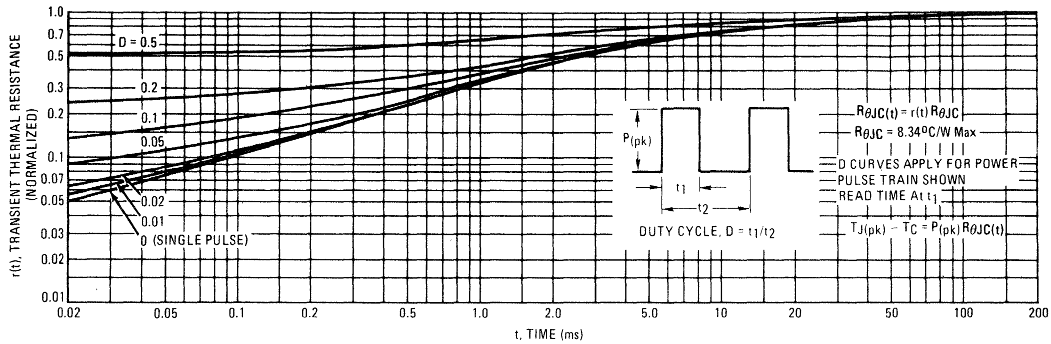
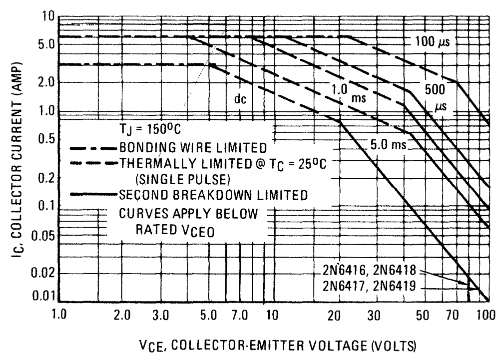


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

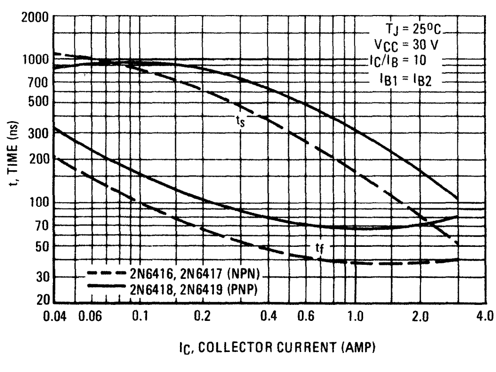
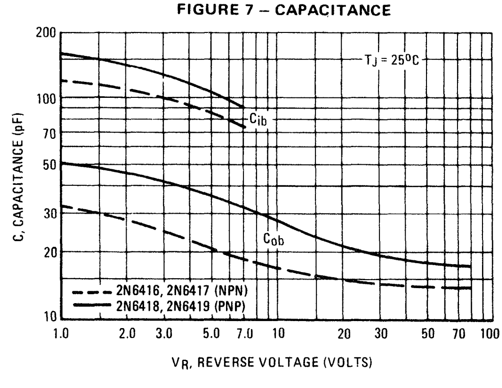


FIGURE 7 – CAPACITANCE



NPN 2N6416, 2N6417	PNP 2N6418, 2N6419

FIGURE 8 – DC CURRENT GAIN

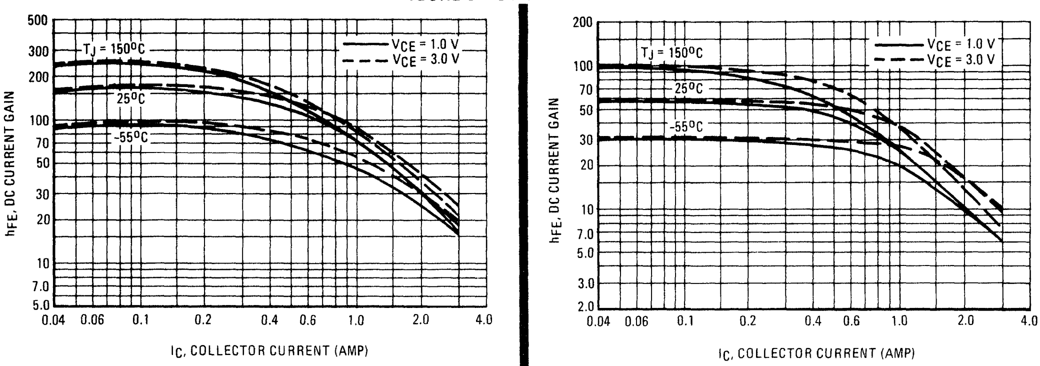


FIGURE 9 – "ON" VOLTAGES

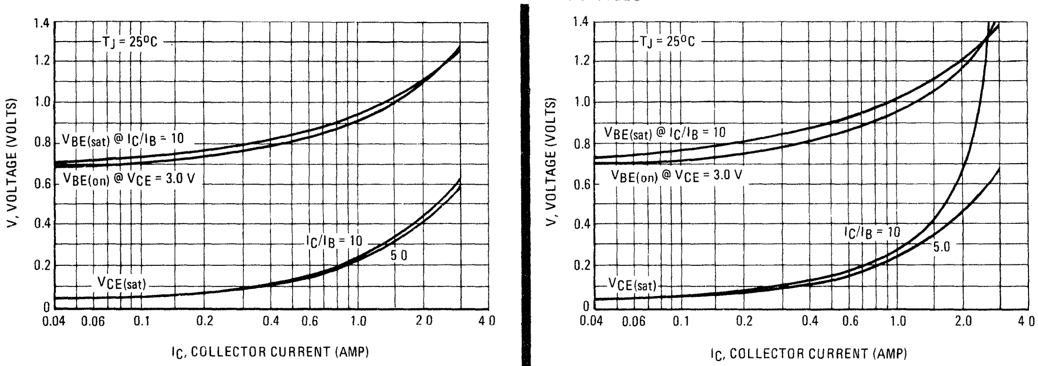
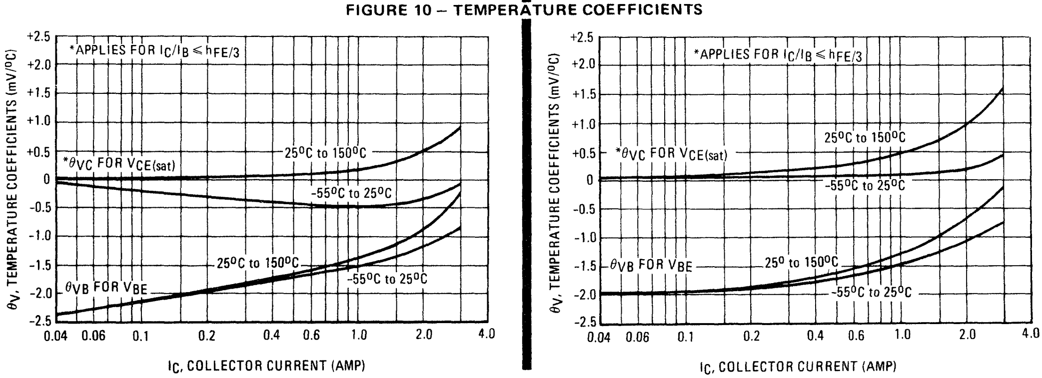


FIGURE 10 – TEMPERATURE COEFFICIENTS



2N6424, 2N6425

For Specifications, See 2N3837 Data, Volume I.