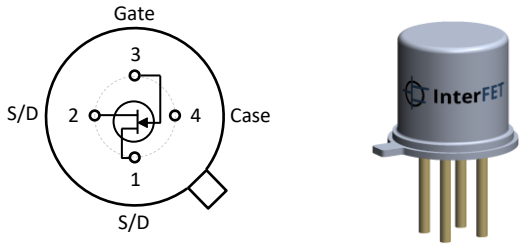
2N6453, 2N6454 N-Channel JFET

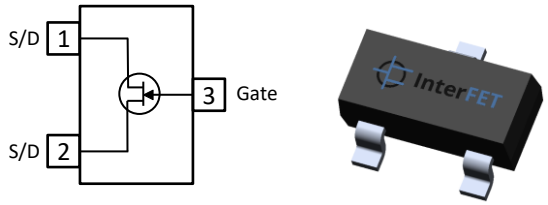
Features

- InterFET N0132L Geometry
- Low noise: 1.0 nV/√Hz typical
- High gain: 32mS typical
- Low gate leakage: 750fA typical @10V
- Typical I_{DSS}: 25mA
- Typical BV_{GSS}: -35V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: InterFET SPICE

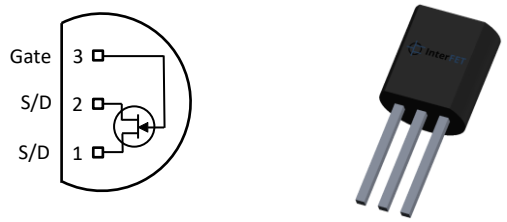
TO-72 Bottom View



SOT23 Top View



TO-92 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections

Industry Standard Crosses

- 2SK152, 2SK170, 2N3972, 2N4393, MMBF4393L
- NSVJ3557SA3, NSVJ5908DSG5, NSVJ2394SA3

InterFET Similar Parts

- IF170D, IFN152
- SMP3972, SMP4393

InterFET Dual Parts

- IF389D, IF1322, IF1322A

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Preamplifiers
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -25V InterFET 2N6453 and 2N6454 are targeted for sensitive amplifier stages for mid-frequencies designs. Gate leakages are typically 750fA at room temperatures. The InterFET proprietary JFET materials and processes result in highest radiation tolerance and lowest leakage JFETs on the market.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N6453; 2N6454	Through-Hole	TO-72	Bulk
PN6453; PN6454	Through-Hole	TO-92	Bulk
SMP6453; SMP6454	Surface Mount	SOT23	Bulk
SMP6453TR; SMP6454TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N6453COT; 2N6454COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N6453CFT; 2N6454CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		TO-72	SOT-23	TO-92	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	-20	-20	V
I_{FG}	Continuous Forward Gate Current	10	10	10	mA
P_D	Continuous Device Power Dissipation[1]	500	350	500	mW
P	Power Derating[1]	3.3	2.8	4	mW/°C
T_J	Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 175	-55 to 150	-55 to 150	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

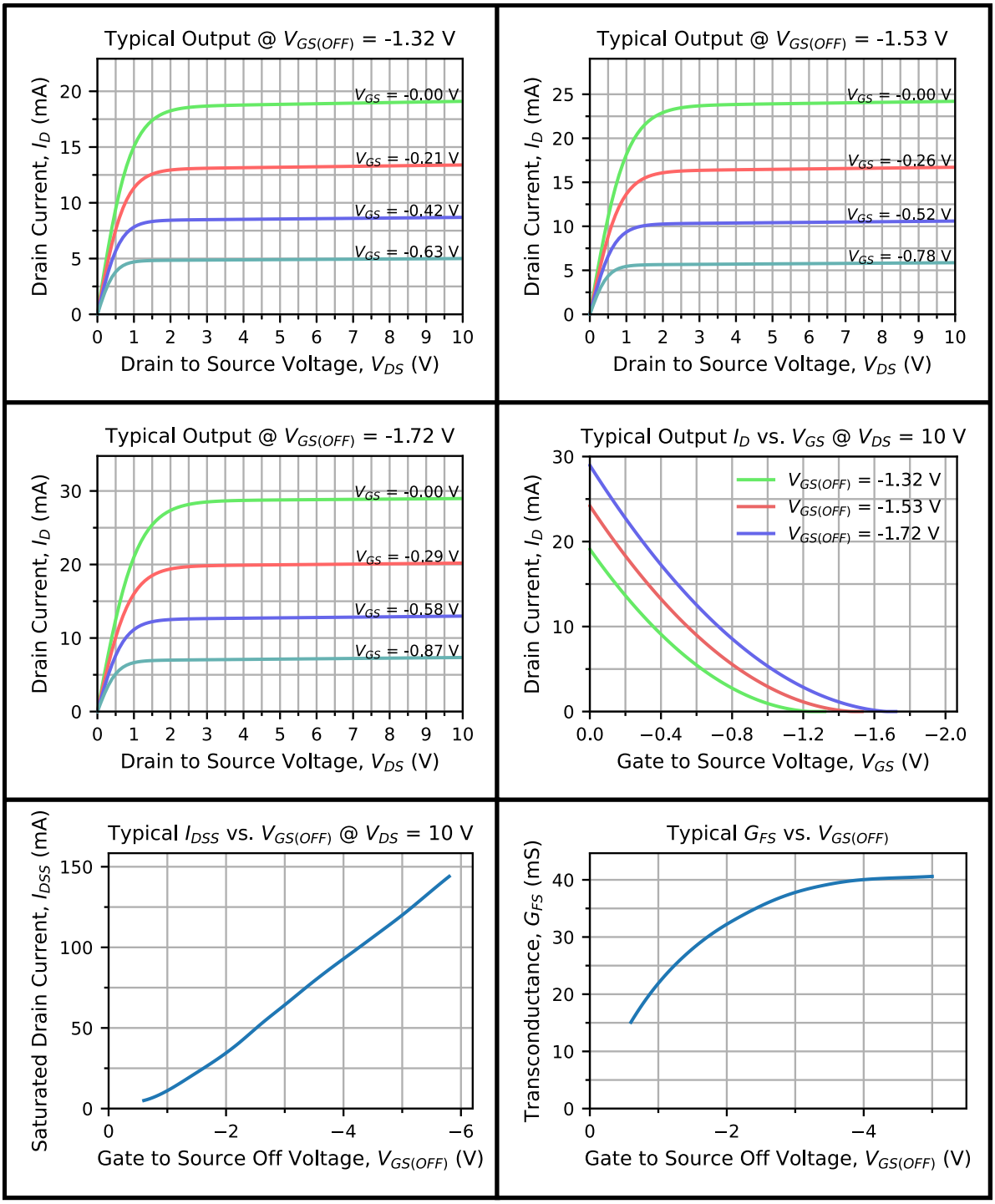
Static Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	2N6453		2N6454		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-20		-25		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -10V, V_{DS} = 0V, T_A = 25°C		-0.1			nA
		V_{GS} = -15V, V_{DS} = 0V, T_A = 25°C				-0.5	
		V_{GS} = -10V, V_{DS} = 0V, T_A = 125°C		-0.2			µA
		V_{GS} = -15V, V_{DS} = 0V, T_A = 125°C				-1	
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 0.5nA	-0.75	-5	-0.75	-5	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 10V (Pulsed)	15	50	15	50	mA

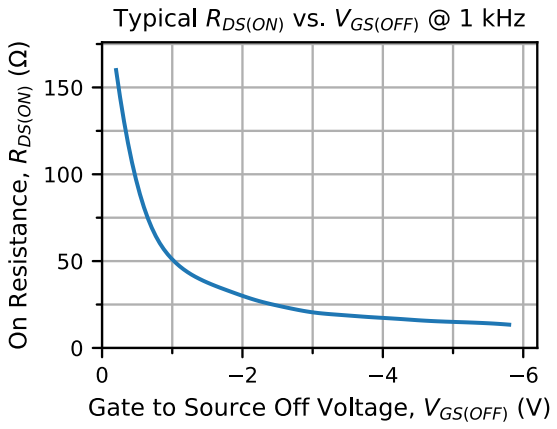
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

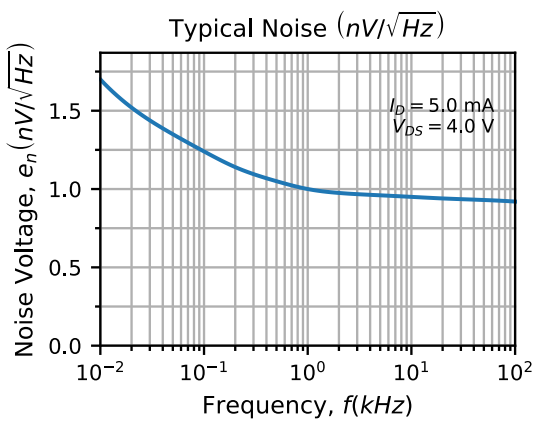
Parameters		Conditions	2N6453		2N6454		Unit
			Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 15mA, f = 1kHz	20	40	20	40	mS
G_{OS}	Output Conductance	V_{DS} = 10V, I_D = 15mA, f = 1kHz		100		100	µS
C_{iss}	Input Capacitance	V_{DS} = 10V, I_D = 15mA, f = 1MHz		25		25	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10V, I_D = 15mA, f = 1MHz		5		5	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 5mA, f = 10Hz V_{DS} = 10V, I_D = 5mA, f = 1kHz		5 3		10 8	nV/√Hz
NF	Noise Figure	V_{DS} = 10V, I_D = 5mA, f = 10Hz R_G = 10 kΩ		1.5		2.5	dB

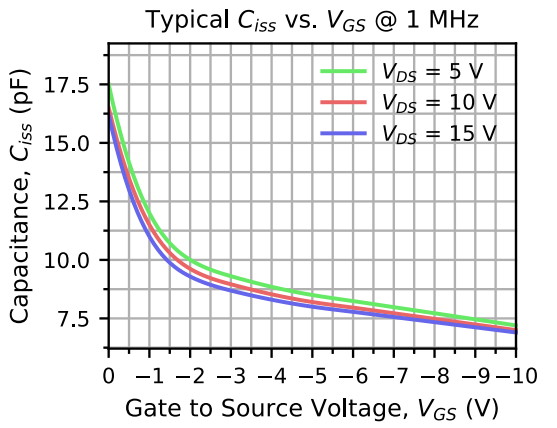
Typical 2N6453, 2N6454 Characteristics

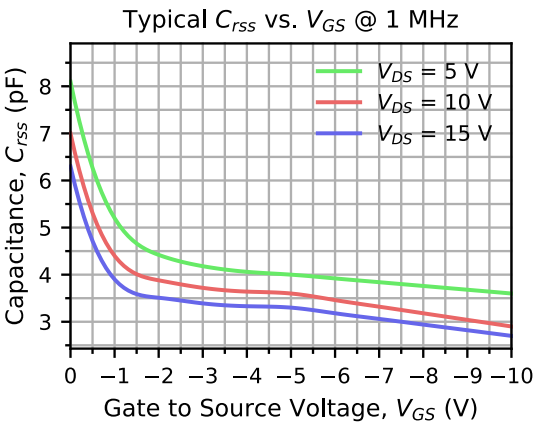


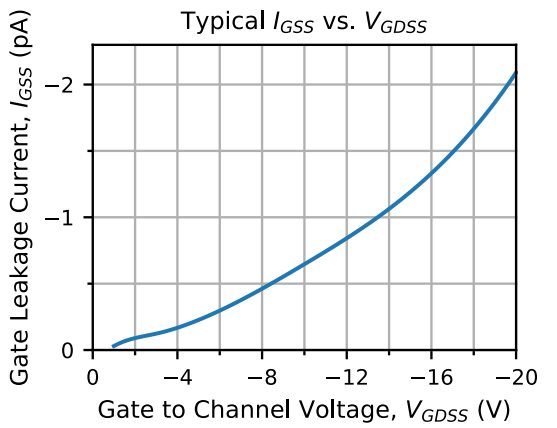
Typical 2N6453, 2N6454 Characteristics (Continued)





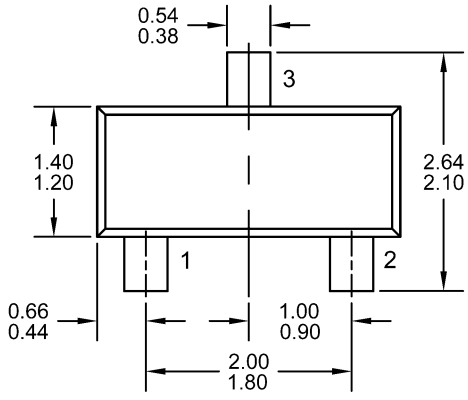


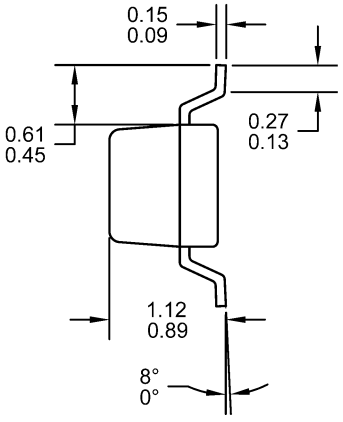


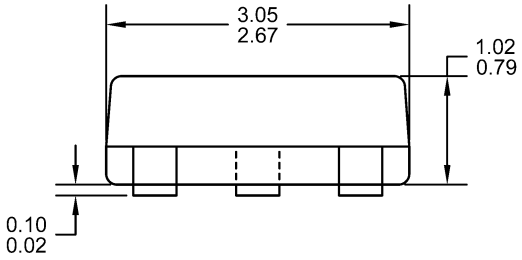


SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

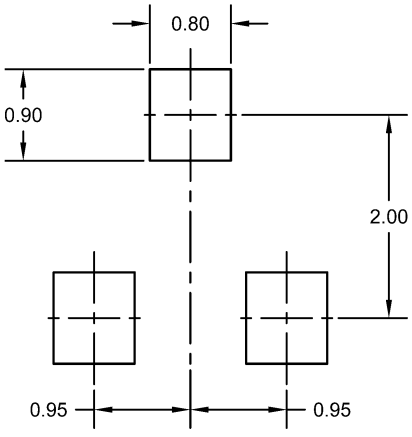






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

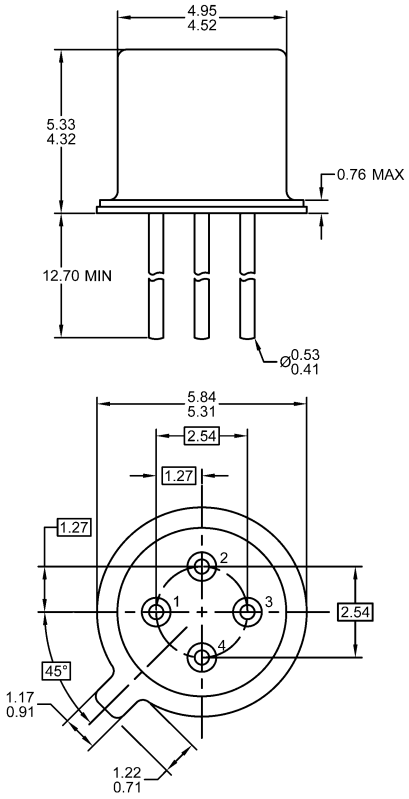
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

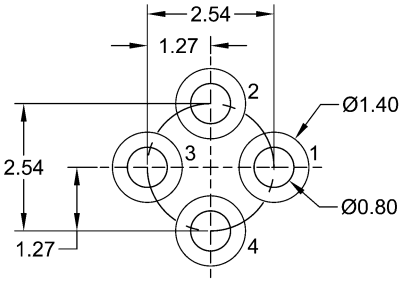
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

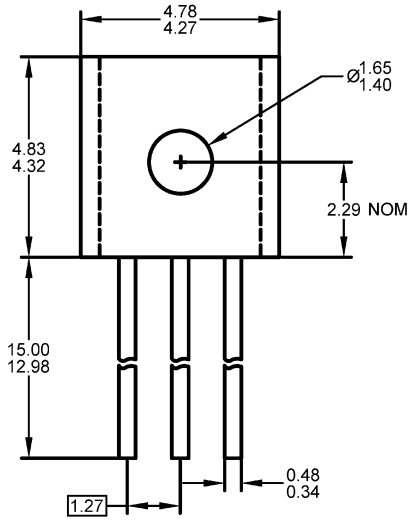
Suggested Through-Hole Layout

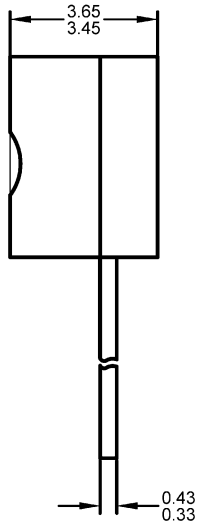


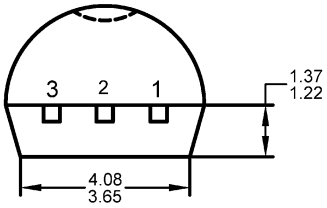
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

TO-92 Mechanical and Layout Data

Package Outline Data

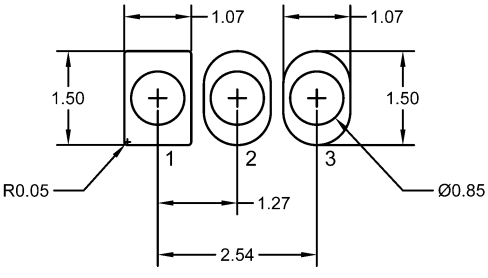






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM

Legal Notice

InterFET Corporation reserves the right to make corrections, enhancements, improvements, modifications, and other changes to its semiconductor products without further notice to this document and any product described herein. InterFET does not assume any liability arising out of the application or use of this document or any product described herein. Unless InterFET has explicitly designated an individual product as meeting the requirements of a particular industry standard, InterFET is not responsible for any failure to meet such industry standard requirements.

InterFET Corporation assumes no liability for a customers product design or applications. Corporate designers and others who are developing systems that incorporate InterFET products understand and agree that they remain responsible for using their independent analysis, evaluation and judgment in designing their applications. Corporate designers and others have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications with all applicable regulations, laws and other applicable requirements.

InterFET Corporation resources are provided "as is" with potential faults. InterFET disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any widespread failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights. InterFET shall not be liable for and shall not defend or indemnify designer against any claim, including but not limited to any infringement claim that relates to or is based on any combination of products even if described in InterFET resources or otherwise. In no event shall InterFET be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of InterFET resources or use thereof, and regardless of whether InterFET has been advised of the possibility of such damages.