

2N6483-2N6485 Low Noise Dual Monolithic N-Channel JFET

FEATURES

- Ultra Low Noise
 $\bar{e}_n < 10 \text{ nV}/\sqrt{\text{Hz}}$ at 10 Hz
- High CMRR > 100 dB
- Low Offset
 $\Delta |V_{GS1} - V_{GS2}| < 5 \text{ mV}$
- Tight Tracking
 $\Delta |V_{GS1} - V_{GS2}| / \Delta T < 5 \mu\text{V}/^\circ\text{C}$

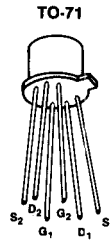
ABSOLUTE MAXIMUM RATINGS (Note 1)
(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C

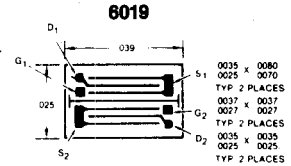
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C

Maximum Voltages & Currents	
V _{GS} Gate to Source Voltage	-50 V
V _{GD} Gate to Drain Voltage	-50 V
V _{G1 G2} Gate to Gate Voltage	±50 V
I _G Gate Current	50 mA

PIN CONFIGURATION



CHIP TOPOGRAPHY



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ORDERING INFORMATION

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I _{GSS}	Gate Reverse Current		200	nA	V _{GS} = -30 V, V _{DS} = 0, T _A = +25°C
			200	nA	V _{GS} = 30 V, V _{DS} = 0, T _A = +150°C
BV _{GSS}	Gate Source Breakdown Voltage	50		V	I _G = 1 μA, V _{DS} = 0
V _p	Gate Source Pinch-Off Voltage	0.7	4.0	V	V _{DS} = 20 V, I _D = 1 nA
I _{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	V _{DS} = 20 V, V _{GS} = 0 (Note 2)
g _{fs}	Common Source Forward Transconductance	1000	4000	μmho	V _{DS} = 20 V, V _{GS} = 0, f = 1 KHz (Note 2)
g _{oss}	Common Source Output Conductance		10	μmho	V _{DS} = 20 V, V _{GS} = 0, f = 1 KHz
C _{iss}	Common Source Input Capacitance		20	pF	V _{DS} = 20 V, V _{GS} = 0, f = 1 MHz
C _{rss}	Common Source Reverse Transfer Capacitance		3.5	pF	V _{DS} = 20 V, V _{GS} = 0, f = 1 MHz
I _G	Gate Current		100	μA	V _{GD} = 20 V, I _D = 200 μA, T _A = +25°C
			100	nA	V _{GD} = 20 V, I _D = 200 μA, T _A = +150°C
V _{GS}	Gate Source Voltage	0.2	3.8	V	V _{DG} = 20 V, I _D = 200 μA
g _{fs}	Common Source Forward Transconductance	500	1500	μmho	V _{DG} = 20 V, I _D = 200 μA, f = 1 KHz (Note 2)
g _{os}	Common Source Output Conductance		1	μmho	V _{DG} = 20 V, I _D = 200 μA
e _n	Equivalent Input Noise Voltage		10	nV/√Hz	V _{DS} = 20 V, I _D = 200 μA, f = 10 Hz
			5	nV/√Hz	V _{DS} = 20 V, I _D = 200 μA, f = 1 KHz

MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

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SYMBOL	CHARACTERISTIC	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1	-	$V_{DS} = 20\text{ V}, V_{GS} = 0$ (Note 2)
$ I_{G1} - I_{G2} $	Differential Gate Current		10		10		10	nA	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$ $T_A = +125^\circ\text{C}$
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	-	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$ $f = 1\text{ KHz}$ (Note 2)
$ g_{os1} - g_{os2} $	Differential Output Conductance		0.1		0.1		0.1	μmho	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$ $f = 1\text{ KHz}$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		5		10		15	mV	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$ $T_A = +25^\circ\text{C}$ to $+125^\circ\text{C}$
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 20\text{ V}, I_D = 200\text{ }\mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+25^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	100		100		90		dB	$V_{DD} = 10$ to 20 V $I_D = 200\text{ }\mu\text{A}$ (Note 3)

- NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
 2. Pulse duration of 2 ms used during test.
 3. $CMRR = 20\text{Log}_{10} \Delta V_{DD} / \Delta|V_{GS1} - V_{GS2}|$, ($\Delta V_{DD} = 10\text{ V}$), not included in JEDEC registration

TYPICAL OPERATING CHARACTERISTICS

