

Transistor, NPN

T0-3



Description:

The 2N6547 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220V line operated switch-mode applications.

Features:

- High temperature performance specified for:
 - Reversed biased SOA with inductive loads.
 - Switching time with inductive loads.
 - Saturation voltages.
 - Leakage currents.

Applications:

Switching regulators.
 PWM inverters and motor controls.
 Solenoid and relay drivers.
 Deflection circuits.

Maximum Ratings

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(SUS)}$	400	V DC
Collector-Emitter Voltage	$V_{CEX(SUS)}$	450	
Collector-Emitter Voltage	V_{CEV}	850	
Emitter-Base Voltage	V_{EB}	9	
Collector Current - Continuous	I_C	15	A DC
Collector Current - Peak	I_{CM}	30	
Base Current - Continuous	I_B	10	
Base Current - Peak	I_{BM}	20	
Emitter Current - Continuous	I_E	25	
Emitter Current - Peak	I_{EM}	35	
Total Power Dissipation at $T_C = 25^\circ\text{C}$ at $T_C = 100^\circ\text{C}$ Derate above 25°C	P_D	175 100 1	W W/°C
Operating and Storage Junction Temperature Range	$T_J T_{stg}$	-65 to +200	°C

Thermal Characteristics

Characteristics	Symbol	Max.	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1	°C/W
Max. Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	°C



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Electrical Characteristics (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
Off Characteristics (1)				
Collector-Emitter Sustaining Voltage ($I_C = 100\text{mA}$, $I_B = 0$)	$V_{EO(sus)}$	400	-	V DC
Collector-Emitter Sustaining Voltage ($I_C = 8\text{A}$, $V_{clamp} = \text{Rated } V_{CEX}$, $T_C = 100^\circ\text{C}$) ($I_C = 15\text{A}$, $V_{clamp} = \text{Rated } V_{CEO} = 100\text{V}$, $T_C = 100^\circ\text{C}$)	$V_{CEX(sus)}$	450 300	-	
Collector Cut off Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{V DC}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{V DC}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	-	1 4	mA DC
Collector Cut off Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	-	5	
Emitter Cut off Current ($V_{EB} = 9\text{V DC}$, $I_C = 0$)	I_{ERO}	-	1	
Second Breakdown				
Second Breakdown Collector Current with Base Forward Biased $t = 1\text{s}$ (Non-repetitive) ($V_{CE} = 100\text{V DC}$)	$I_{S/b}$	0.2	-	A DC
On Characteristic (1)				
DC Current Gain ($I_C = 5\text{A DC}$, $V_{CE} = 2\text{V DC}$) ($I_C = 10\text{A DC}$, $V_{CE} = 2\text{V DC}$)	h_{FE}	12 6	60 30	-
Collector-Emitter Saturation Voltage ($I_C = 10\text{A DC}$, $I_B = 2\text{A DC}$) ($I_C = 15\text{A DC}$, $I_B = 3\text{A DC}$) ($I_C = 10\text{A DC}$, $I_B = 2\text{A DC}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	-	1.5 5 2.5	V DC
Base-Emitter Saturation Voltage ($I_C = 10\text{A DC}$, $I_B = 2\text{A DC}$) ($I_C = 10\text{A DC}$, $I_B = 2\text{A DC}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	-	1.6	
Dynamic Characteristics				
Current-Gain-Bandwidth Product ($I_C = 500\text{mA DC}$, $V_{CE} = 10\text{V DC}$, $f_{test} = 1\text{MHz}$)	f_T	6	28	MHz
Output Capacitance ($V_{CB} = 10\text{V DC}$, $I_E = 0$, $f_{test} = 1\text{MHz}$)	C_{ob}	125	500	pF

Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

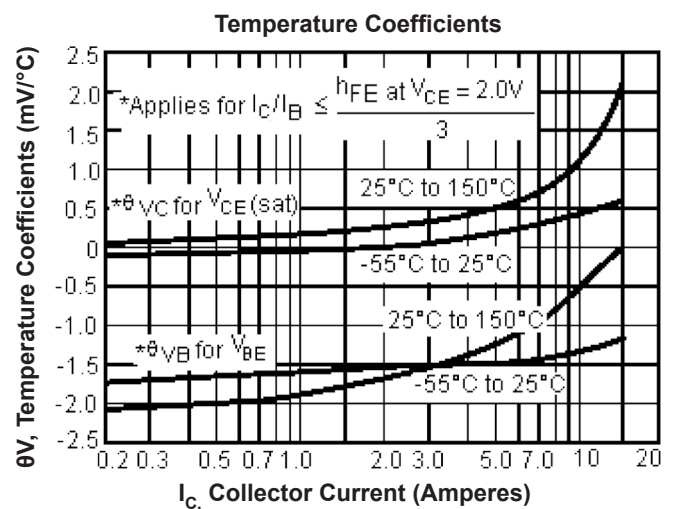
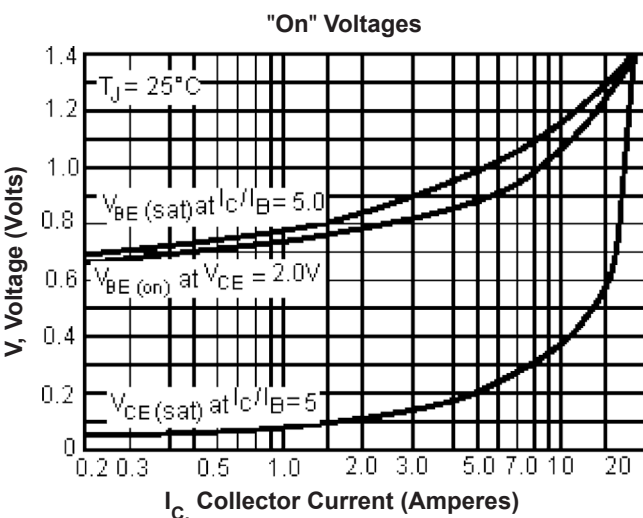
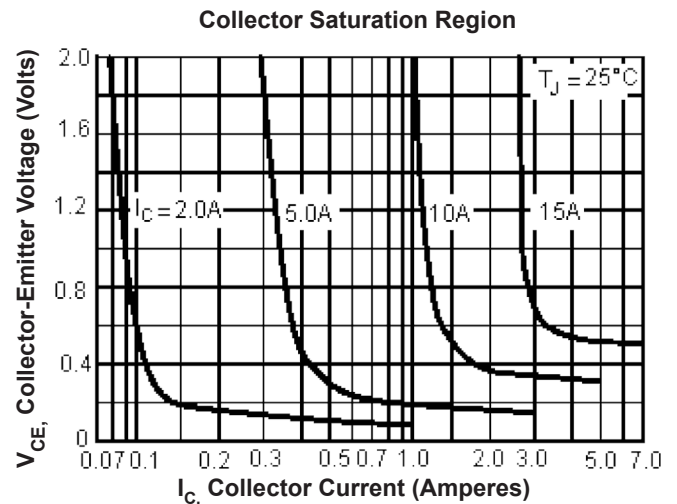
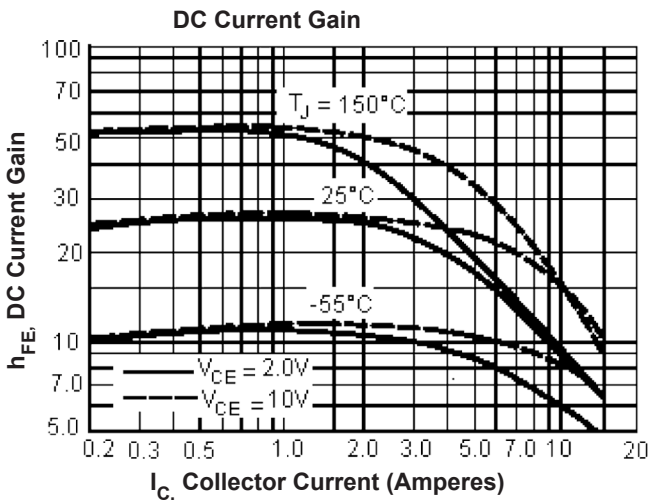
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Switching Characteristics

Resistive Load					
Delay Time	$(V_{CC} = 250V, I_C = 10A, I_{B1} = I_{B2} = 2A, t_p = 100\mu S, \text{Duty Cycle} \leq 2\%)$	t_d	-	0.05	μs
Rise Time		t_r	-	1	
Storage Time		t_s	-	4	
Fall Time		t_f	-	0.7	
Inductive Load, Clamped					
Storage Time	$(I_C = 10A (pk), V_{clamp} = \text{Rated } V_{CEX}, I_{B1} = 2A, V_{BE(off)} = 5V \text{ DC}, T_C = 100^\circ C)$	t_s	-	5	μs
Fall Time		t_f	-	1.5	
Storage Time	$(I_C = 10A (pk), V_{clamp} = \text{Rated } V_{CEX}, I_{B1} = 2A, V_{BE(off)} = 5V \text{ DC}, T_C = 25^\circ C)$	t_s	Typical 2		μs
Fall Time		t_f	Typical 0.09		

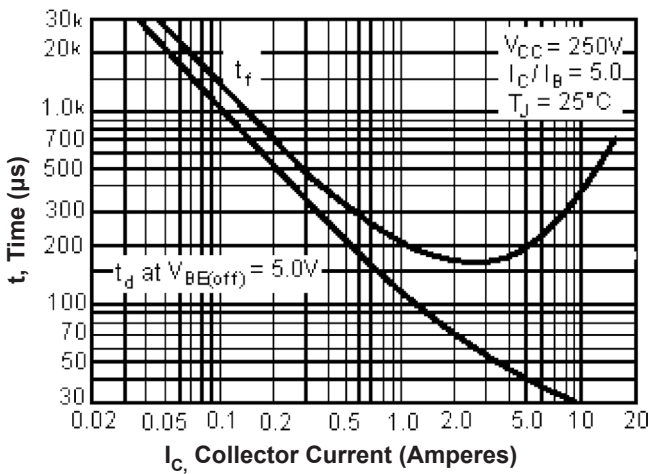
Typical Electrical Characteristics



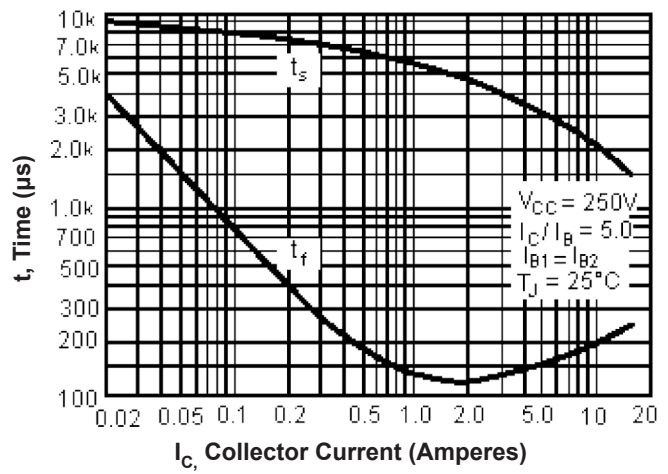
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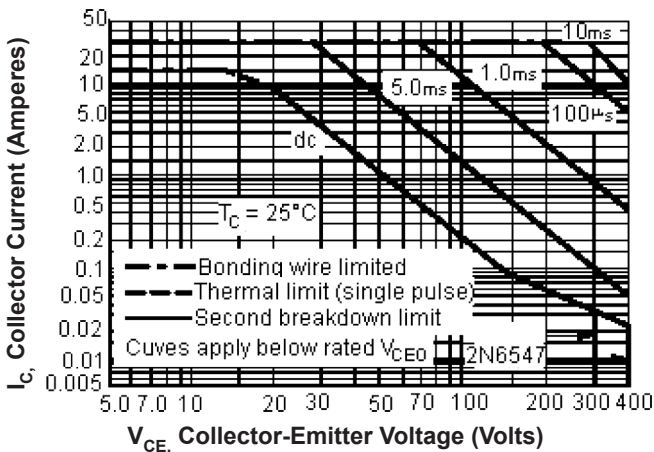
Turn-On Time



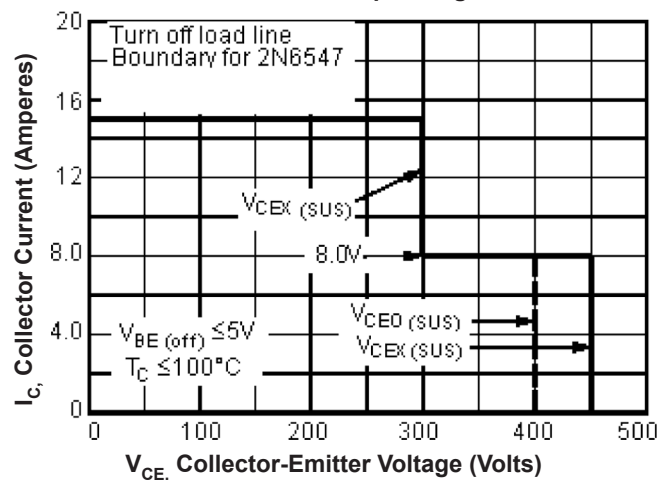
Turn-Off Time



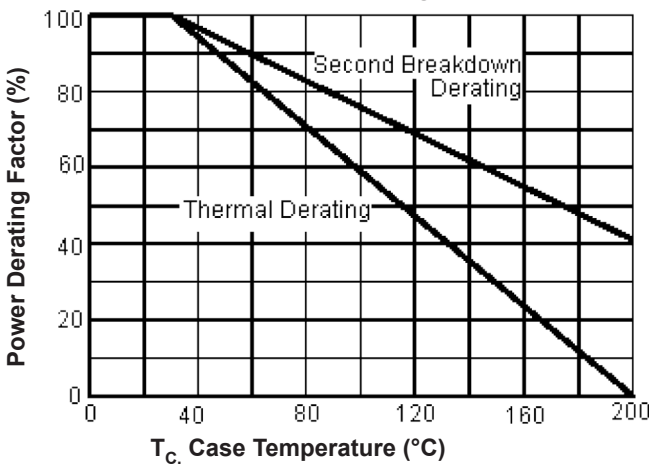
Forward Bias Safe Operating Area



Reverse Bias Safe Operating Area



Power Derating



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

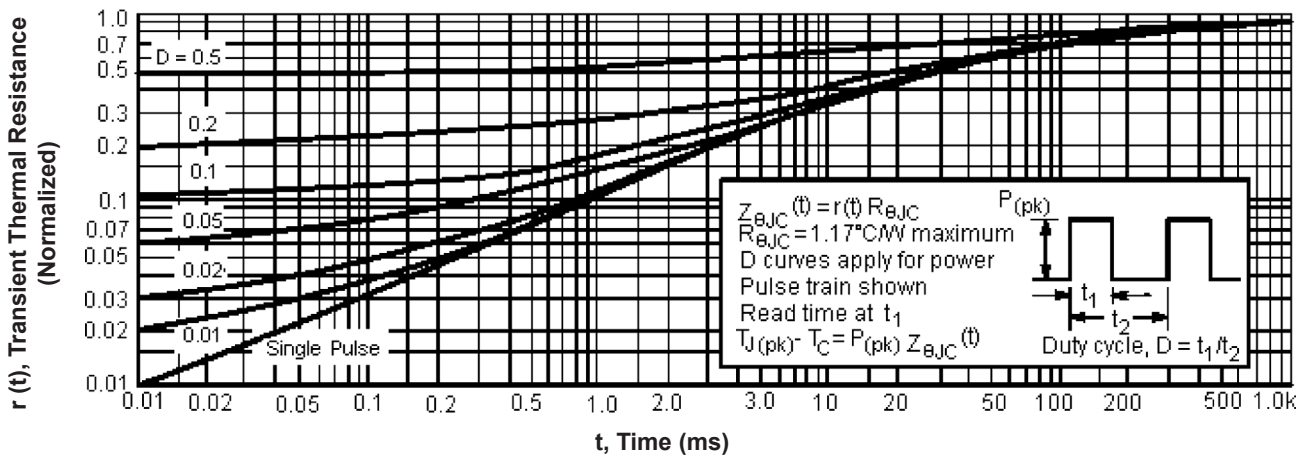
The data is based on $T_C = 25^\circ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown may be found at any case temperature by using the appropriate curve. $T_{J(pk)}$ may be calculated from the data. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



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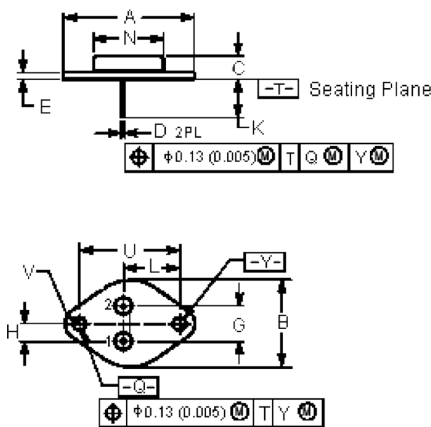


Thermal Response



Dimensions

TO-204 (TO-3)



Dim.	Min.	Max.
A	1.55 (39.37)	Reference
B	-	1.05 (26.67)
C	0.25 (6.35)	0.335 (8.51)
D	0.038 (0.97)	0.043 (1.09)
E	0.055 (1.4)	0.07 (1.77)
G	0.43 (10.92)	BSC
H	0.215 (5.46)	BSC
K	0.44 (11.18)	0.48 (12.19)
L	0.665 (16.89)	BSC
N	-	0.83 (21.08)
Q	0.151 (3.84)	0.165 (4.19)
U	1.187 (30.15)	BSC
V	0.131 (3.33)	0.188 (4.77)

Dimensions : Inches (Millimetres)

Pin Configuration

- Pin 1. Base
- 2. Emitter
- Collector (Case)

Part Number Table

Description	Part Number
Transistor, NPN, TO-3	2N6547

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