

**REPETITIVE AVALANCHE AND dv/dt RATED
HEXFET[®] TRANSISTORS
THRU-HOLE (TO-204AA/AE)**

**IRF9130
JANTX2N6804
JANTXV2N6804
[REF:MIL-PRF-19500/562]
100V, P-CHANNEL**

Product Summary

Part Number	BVDSS	RDS(on)	ID
IRF9130	-100V	0.30 Ω	-11A



TO-3

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling

Absolute Maximum Ratings

	Parameter		Units
ID @ VGS = 0V, TC = 25°C	Continuous Drain Current	-11	A
ID @ VGS = 0V, TC = 100°C	Continuous Drain Current	-7.0	
IDM	Pulsed Drain Current ①	-50	
PD @ TC = 25°C	Max. Power Dissipation	75	W
	Linear Derating Factor	0.60	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	81	mJ
IAR	Avalanche Current ①	-11	A
EAR	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5 (typical)	g

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-100	—	—	V	VGS = 0V, ID = -1.0mA
ΔBVDSS/ΔTj	Temperature Coefficient of Breakdown Voltage	—	-0.087	—	V/°C	Reference to 25°C, ID = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.30	Ω	VGS = -10V, ID = -7.0A④
		—	—	0.35		VGS = -10V, ID = -11A ④
VGS(th)	Gate Threshold Voltage	-2.0	—	-4.0	V	VDS = VGS, ID = -250μA
gfs	Forward Transconductance	3	—	—	S (Ω)	VDS > 15V, IDS = -7.0A④
IDSS	Zero Gate Voltage Drain Current	—	—	-25	μA	VDS = -80V, VGS = 0V
		—	—	-250		VDS = -80V VGS = 0V, Tj = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	-100	nA	VGS = -20V
IGSS	Gate-to-Source Leakage Reverse	—	—	100	nA	VGS = -20V
Qg	Total Gate Charge	—	—	29	nC	VGS = -10V, ID = -11A VDS = -50V
Qgs	Gate-to-Source Charge	—	—	7.1		
Qgd	Gate-to-Drain ('Miller') Charge	—	—	21		
td(on)	Turn-On Delay Time	—	—	60	ns	VDD = -50V, ID = -11A, RG = 7.5Ω
tr	Rise Time	—	—	140		
td(off)	Turn-Off Delay Time	—	—	140		
tf	Fall Time	—	—	140		
LS + LD	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
Ciss	Input Capacitance	—	860	—	pF	VGS = 0V, VDS = 25V f = 1.0MHz
Coss	Output Capacitance	—	350	—		
Crss	Reverse Transfer Capacitance	—	125	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
IS	Continuous Source Current (Body Diode)	—	—	-11	A	
ISM	Pulse Source Current (Body Diode) ①	—	—	-50		
VSD	Diode Forward Voltage	—	—	-4.7	V	Tj = 25°C, IS = -11A, VGS = 0V ④
trr	Reverse Recovery Time	—	—	250	nS	Tj = 25°C, IF = -11A, di/dt ≤ 100A/μs
QRR	Reverse Recovery Charge	—	—	3.0	μc	VDD ≤ -50V ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
RthJC	Junction to Case	—	—	1.67	°C/W	soldered to a 2" square copper-clad board
RthJA	Junction-to-Ambient	—	—	30		

For footnotes refer to the last page

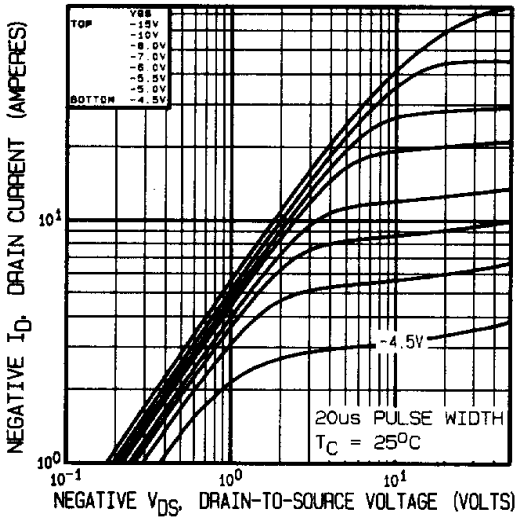


Fig 1. Typical Output Characteristics

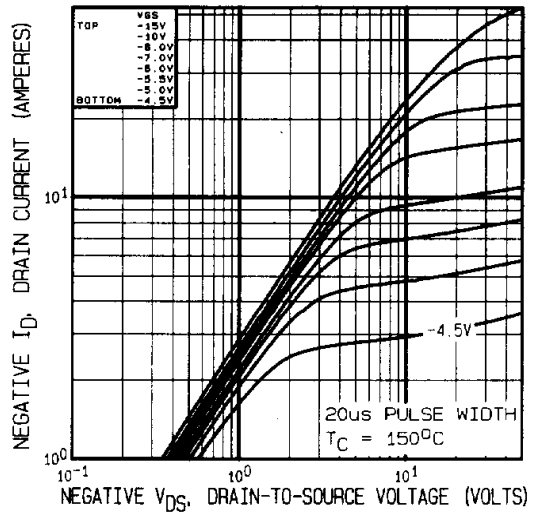


Fig 2. Typical Output Characteristics

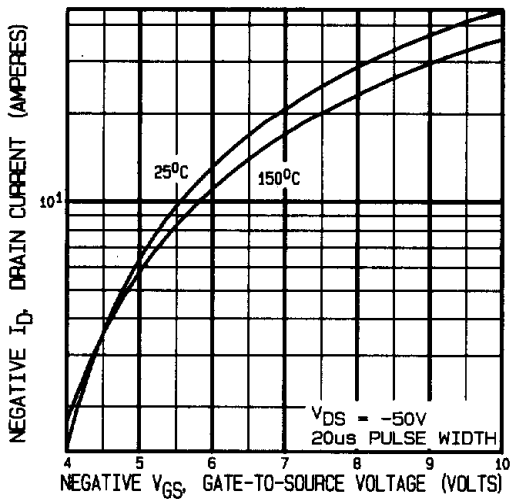


Fig 3. Typical Transfer Characteristics

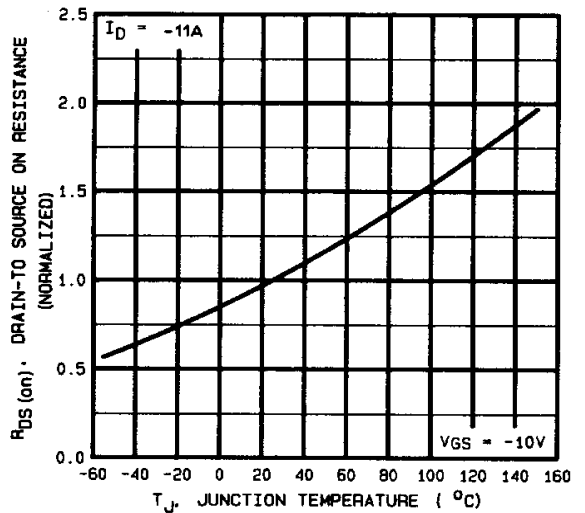


Fig 4. Normalized On-Resistance Vs. Temperature

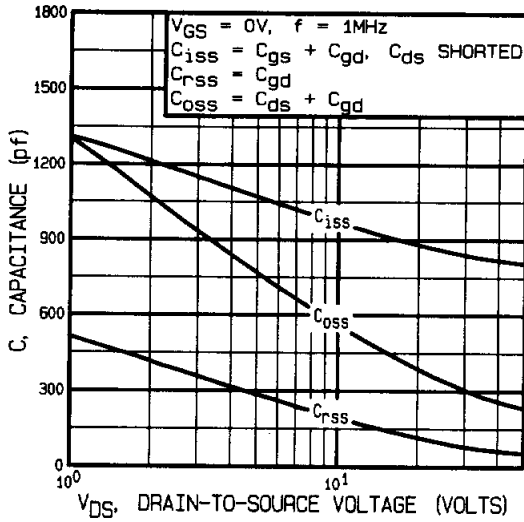


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

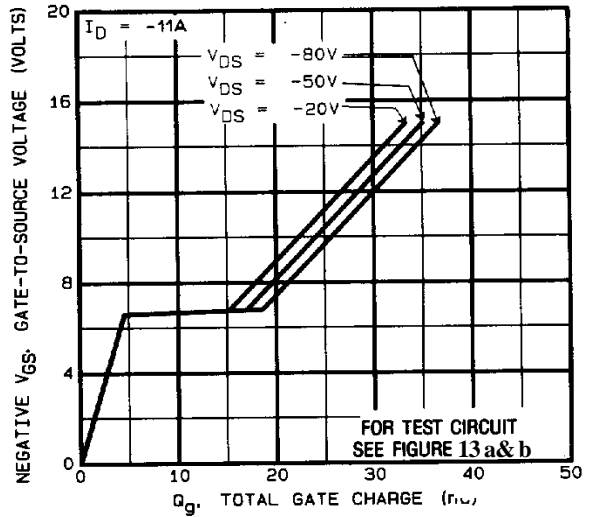


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

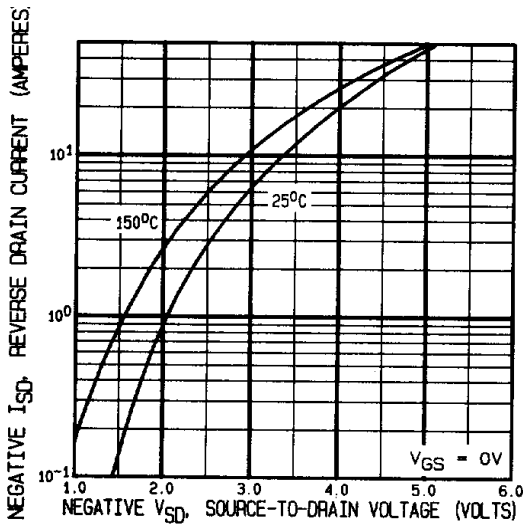


Fig 7. Typical Source-Drain Diode Forward Voltage

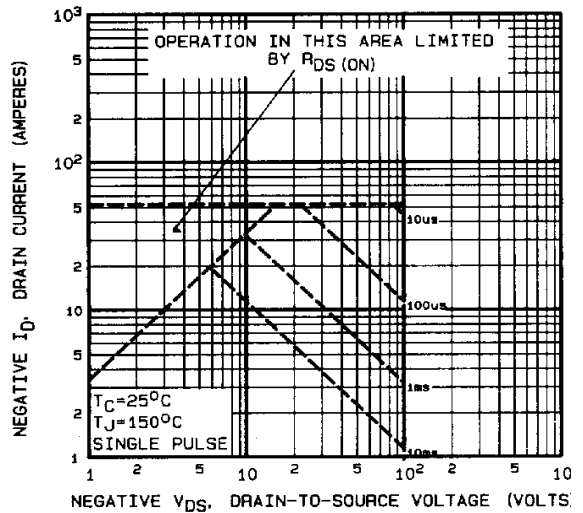


Fig 8. Maximum Safe Operating Area

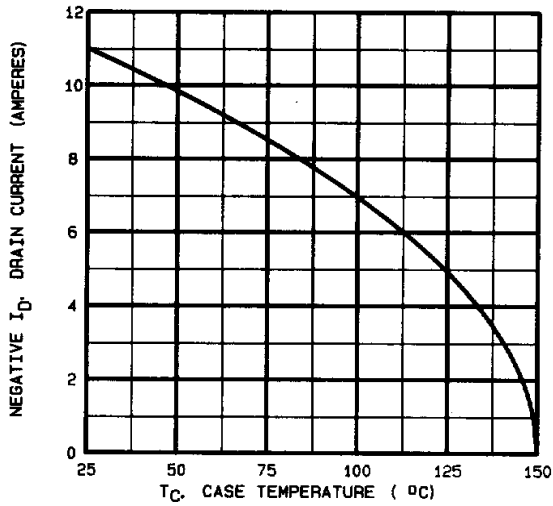


Fig 9. Maximum Drain Current Vs. Case Temperature

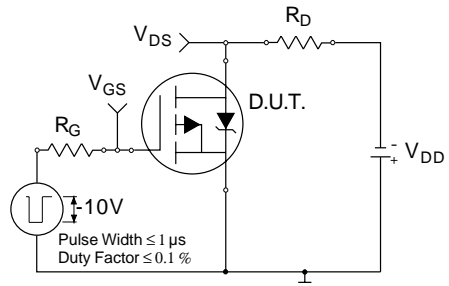


Fig 10a. Switching Time Test Circuit

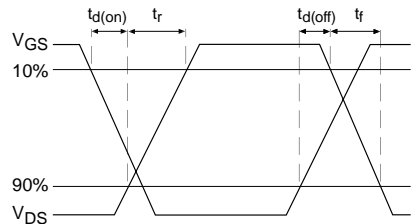


Fig 10b. Switching Time Waveforms

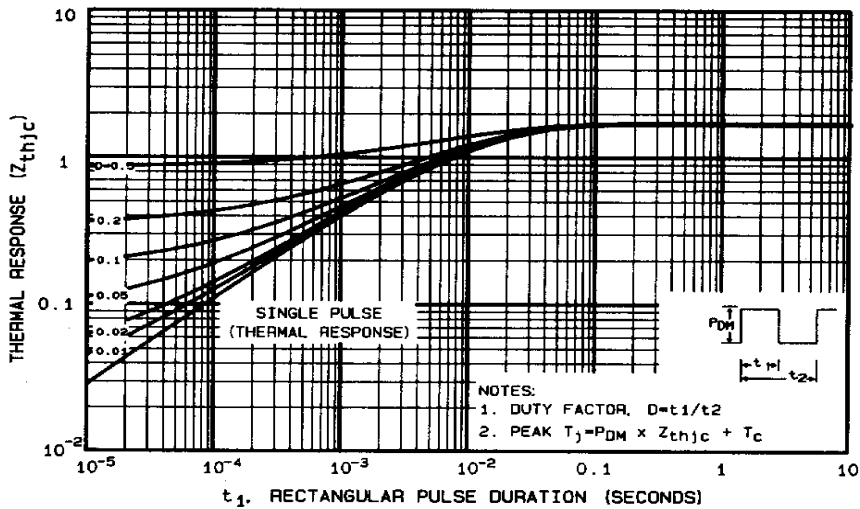


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

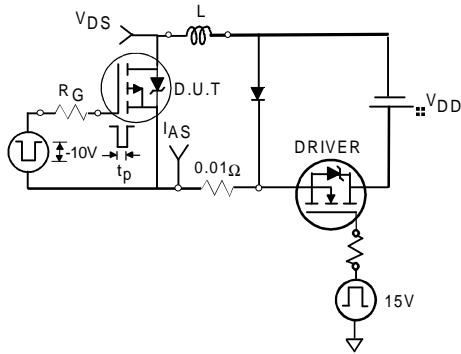


Fig 12a. Unclamped Inductive Test Circuit

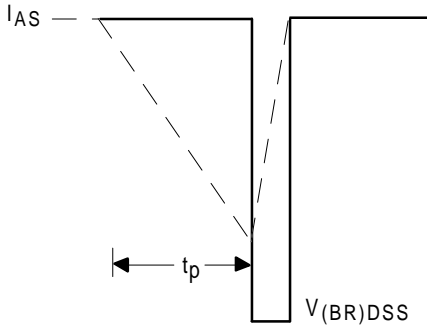


Fig 12b. Unclamped Inductive Waveforms

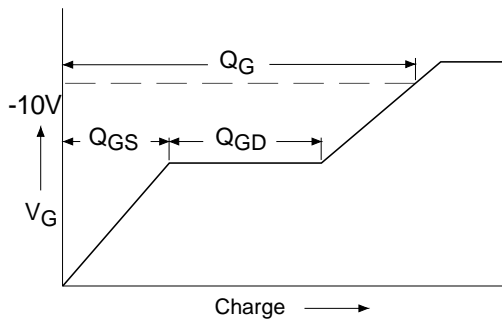


Fig 13a. Basic Gate Charge Waveform

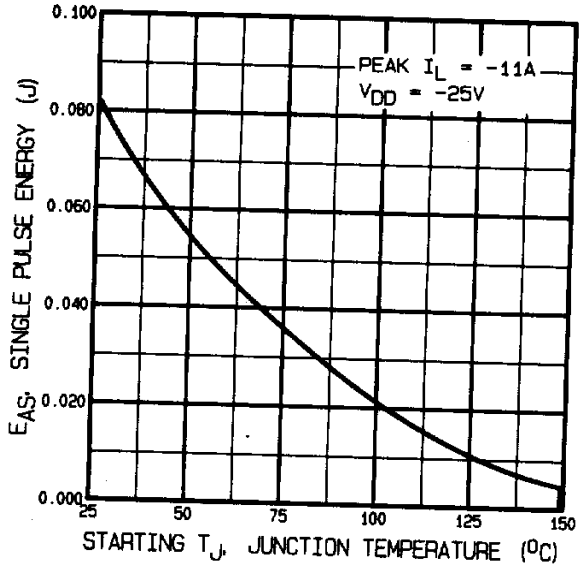


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

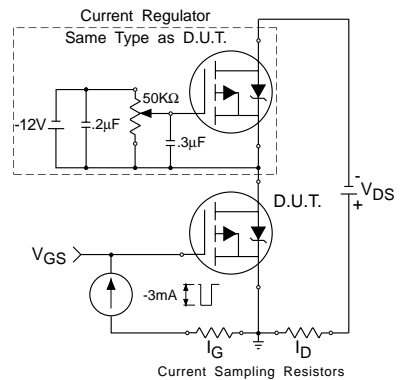
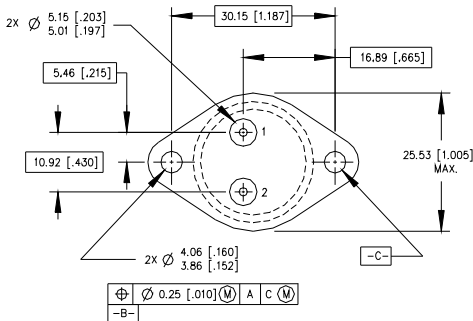
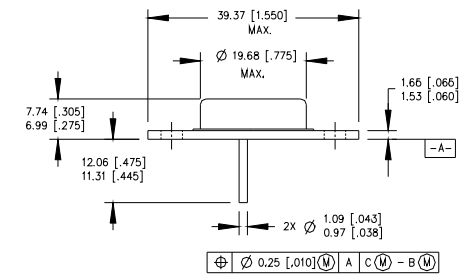


Fig 13b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^{\circ}C$,
Peak $I_L = -11A$,
- ③ $I_{SD} \leq 11A$, $di/dt \leq 140A/\mu s$,
 $V_{DD} \leq -100V$, $T_J \leq 150^{\circ}C$
Suggested $R_G = 7.5 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —TO-204AA (Modified TO-3)



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204-AA.