2N6908 SERIES

Siliconix incorporated

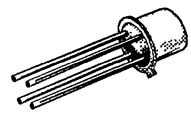
N-Channel JFET Circuits

The 2N6908 Series is much more than a JFET. The addition of back-to-back diodes effectively clamps input "over-voltage" while a high-performance JFET provides an effective amplification stage. With the addition of a source resistor, a complete common-source amplifier is created which provides both low leakage and very low noise. This performance is especially effective as a small signal pre-amplifier as well as impedance matching between low and high impedance sources. Finally, its TO-72 package is hermetically sealed and is available with full military screening per MIL-S-19500. (See Section 1.)

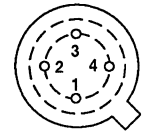
For additional design information please see performance curves NBB, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (μS)	I_{DSS} MAX (mA)
2N6908	-1.8	-30	100	2
2N6909	-2.3	-30	400	3.5
2N6910	-3.5	-30	1200	5

TO-72



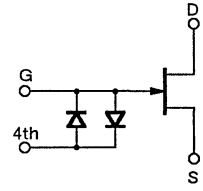
BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE
4 DIODES

SIMILAR PRODUCTS

- SOT-143, See SST6908 Series
- Chips, Order 2N69XXCHP



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Forward Gate Current	I_G	10	mA
Power Dissipation	P_D	300	mW
Power Derating		2.4	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				2N6908		2N6909		2N6910		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA, V_{DS} = 0 V, V_{G4} = 0 V	−50	−30		−30		−30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA, V_{G4} = 0 V		−0.3	−1.8	−0.6	−2.3	−0.9	−3.5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V, V_{G4} = 0 V		0.05	2	0.2	3.5	0.6	5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −15 V, V_{DS} = 0 V, V_{G4} = 0 V	−2		−25		−25		−25	pA
		T_A = 125°C	−1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 50 µA	−2							pA
Forward Gate Diode Current[4]	I_{G4}	V_{G4} = ± 100 mV	± 1		± 10		± 10		± 10	pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = ± 0.5 mA, V_{DS} = 0 V, V_{G4} = 0 V	± 0.7		± 1.2		± 1.2		± 1.2	V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, V_{G4} = 0 V, f = 1 kHz		0.1	3	0.4	3.5	1.2	4	mS
Common-Source Output Conductance	g_{os}				50		75		100	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, V_{G4} = 0 V, f = 1 MHz	3.2		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		2		2		2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	12		25		25		25	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ	0.1		1		1		1	dB

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Forward diode current when a voltage is applied between gate and fourth lead.

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