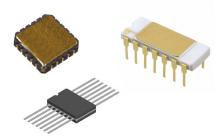


Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Features

- Available in JAN, JANTX, JANTXV and JANS per MIL-PRF-19500/558
- TO-116, 20 PIN Leadless (U) and 14 PIN Flat Pack package types
- Radiation Tolerant Levels M, D, P, L, and R



Electrical Characteristics

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Off Characteristics					
Collector - Emitter Breakdown Voltage	I _C = 10 mA dc	$V_{(BR)CEO}$	V dc	60	_
Collector - Base Cutoff Current	V_{CB} = 60 V dc V_{CB} = 50 V dc	I _{CBO1}	μΑ dc nA dc	_	10 10
Emitter - Base Cutoff Current	V _{BE} = 5.0 V dc V _{EB} = 4.0 V dc	I _{EBO1}	μA dc nA dc	_	10 50
On Characteristics ¹					
Forward Current Transfer Ratio	V_{CE} = 10 V dc; I_{C} = 0.1 mA dc V_{CE} = 10 V dc; I_{C} = 1.0 mA dc V_{CE} = 10 V dc; I_{C} = 10 mA dc V_{CE} = 10 V dc; I_{C} = 150 mA dc V_{CE} = 10 V dc; I_{C} = 500 mA dc	h _{FE}	-	75 100 100 100 50	450 300
Collector - Emitter Saturation Voltage	$I_{\rm C}$ = 150 mA dc; $I_{\rm B}$ = 15 mA dc $I_{\rm C}$ = 500 mA dc, $I_{\rm B}$ = 50 mA dc	V _{CE(SAT)1} V _{CE(SAT)2}		_	0.4 1.6
Base - Emitter Saturation Voltage	$I_{\rm C}$ = 150 mA dc; $I_{\rm B}$ = 15 mA dc $I_{\rm C}$ = 500 mA dc; $I_{\rm B}$ = 50 mA dc	V _{BE(SAT)1}			1.3 2.6
Dynamic Characteristics		1	'		l
Magnitude of Common Small-Signal Short-Circuit Forward Current Transfer Ratio	V _{CE} = 20 V dc; I _C = 50 mA dc; f = 100 MHz	h _{FE}	-	2.0	8
Small-Signal Short Circuit Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V dc}$; $I_{C} = 1.0 \text{ mA dc}$; $f = 1 \text{ kHz}$	h _{fe}	-	100	_
Open Circuit Output Capacitance	V _{CB} = 10 V dc; I _E = 0; 100 kHz ≤ f ≤ 1 MHz	C _{obo}	pF	_	8.0
Input Capacitance (Output Open-Circuited)	V _{EB} = 2.0 V dc; I _C = 0; 100 kHz ≤ f ≤ 1 MHz	C _{ibo}	pF	_	30

VPT Components and its affiliates reserve the right to make changes to the product(s) or information contained herein without notice.

Visit www.vptcomponents.com for additional data sheets and product information.



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Electrical Characteristics (T_A = +25°C unless otherwise specified)

Parameter	Test Conditions		Units	Min.	Max.	
Collector - Base Cutoff Current	T _A = +150°C V _{CB} = 50 V dc	I _{CBO3}	μA dc	_	10	
Forward-Current Transfer Ratio	$T_A = -55^{\circ}C$ $V_{CE} = 10 \text{ V dc}; I_C = 1.0 \text{ mA dc}$	h _{FE6}		50		
Transistor to Transistor Resistance	V _{T-T} = 500 V dc	R _{T-T}	ohms	10 ¹⁰	_	
Switching Characteristics						
Turn-On Time (saturated)	See figure 13 of MIL-PRF-19500/559	t _{on}	ns	_	45	
Turn-Off Time (saturated)	See figure 14 of MIL-PRF-19500/559	t _{off}	ns	_	300	



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Absolute Maximum Ratings ($T_A = 25^{\circ}C$ unless otherwise specified) ⁽¹⁾

Ratings	Symbol	Value
Collector - Emitter Voltage	V _{CEO (5)}	60 Vdc
Collector - Base Voltage	V _{CBO (5)}	60 Vdc
Emitter - Base Voltage	V _{EBO (5)}	5.0 Vdc
Collector Current	I _{C (3)}	600 mAdc
Total Power Dissipation @ T _A = +25°C 2N6987 2N6987U 2N6988	P _{T (2)}	1.5 W 1.0 W 1.0 W
Total Power Dissipation @ T _{A(AM)} = +25°C 2N6988	P _{T (2)}	1.0 W
Operating & Storage Temperature Range	T _J , T _{STG}	-65°C to +200°C

Thermal Characteristics

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Ambient 2N6987 2N6987U 2N6988	R ₀ JA (3)	85°C/W 160°C/W 175°C/W
Thermal Resistance, Junction to Ambient 2N6987 2N6987U 2N6988	R _{θJA(AM)} (3) (4)	N/A N/A 23°C/W

- (1) Maximum voltage between transistors shall be >500 V dc
- (2) For derating see figures 5, 6, 7 and 8 of MIL-PRF-19500/558
- (3) For thermal impedance graphs, see figures 9, 10, 11 and 12 of MIL-PRF-19500/558.
- (4) Thermally conductive adhesive mount to infinite heat sink
- (5) Ratings apply to each transistor in the array



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Outline Drawing 2N6987

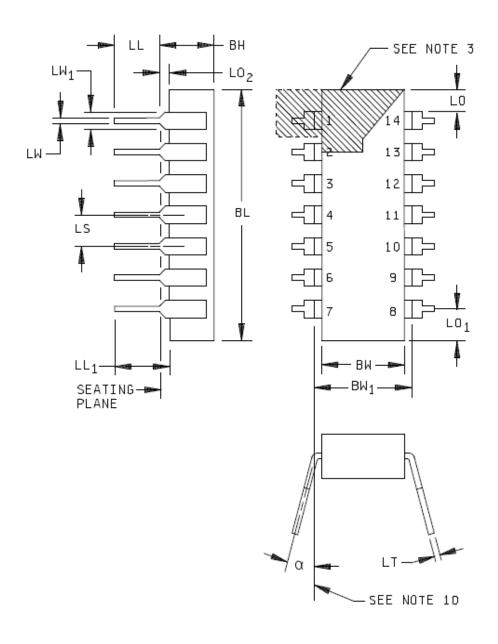


FIGURE 1. Dimensions and configuration for type 2N6987.



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Outline Dimensions 2N6987

Symbol	Inc	hes	Millimeters		Notes
	Min	Max	Min	Max	
ВН		.200		5.08	
LW	.014	.023	0.36	0.58	8
LW ₁	.030	.070	0.76	1.78	4, 8
LT	.008	.015	0.20	0.38	8
BL		.785		19.94	4
BW	.220	.310	5.59	7.87	4
BW ₁	.290	.320	7.37	8.13	7
LS	.100	BSC	2.54	BSC	5, 9
LL	.125	.200	3.18	5.08	
LL ₁	.150		3.81		
LO ₂	.015	.060	0.38	1.52	3
LO ₁		.098		2.49	6
LO	.005		0.13		6
α	0°	15°	0°	15°	

NOTES:

- 1. Dimensions are in inches.
- 2. Millimeters are given for information only.
- Index area; a notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- 4. The minimum limit for dimension LW₁ may be .023 inch (0.58 mm) for lead numbers 1, 7, 8, and 14 only.
- Dimension LO₂ shall be measured from the seating plane to the base plane.
- 6. This dimension allows for off-center lid, meniscus, and glass overrun.
- The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 inch (±0.25 mm) of its exact longitudinal position relative to pins 1 and 14.
- 8. Applies to all four corners (lead numbers 1, 7, 8, and 14).
- 9. Lead center when α is 0 degrees. BW₁ shall be measured at the centerline of the leads.
- All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish A is applied. Pointed or round lead ends are allowed.
- Twelve spaces.
- No organic or polymeric materials shall be molded to the bottom of the package to cover leads.
- 13. For terminal connections, see figure 4.
- In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

FIGURE 1. Dimensions and configuration for type 2N6987 - Continued.



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Outline Drawing 2N6988

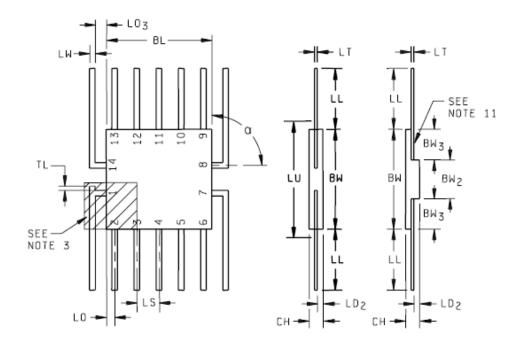


FIGURE 2. Physical dimensions for type 2N6988.



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Outline Dimension 2N6988

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
СН	.030	.115	0.76	2.92	
LW	.010	.019	0.25	0.48	7
TL	.008	.015	0.20	0.38	12
BL		.280		7.11	5
BW	.240	.260	6.10	6.60	
LU		.290		7.37	5
BW ₂	.125		3.18		

Symbol	Inc	nches Millimeters		Inches		Notes
	Min	Max	Min	Max		
BW ₃	.030		0.76			
LS	.050 BSC		1.27 BSC		6, 8	
LT	.003	.006	0.076	0.152	7	
LL	.250	.370	6.35	9.40		
LD ₂	.005	.040	0.13	1.02	4	
LO	.005		0.13		9, 10	
LO ₃	.004		0.10		13	
α	30°	90°	30°	90°	14	

NOTES:

- Dimensions are in inches.
- 2. Millimeters are given for general information only.
- 3. Index area: A notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dim TL) may be used to identify pin one.
- Dimension LD₂ shall be measured at the point of exit of the lead from the body.
- 5. This dimension allows for off-center lid, meniscus, and glass overrun.
- 6. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
- 7. All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat when the lead finish is solder.
- 8. Twelve spaces.
- 9. Applies to all four corners (leads number 2, 6, 9, and 13).
- 10. Dimension LO may be .000 inch (0.00 mm if leads number 2, 6, 9, and 13) bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metallized ceramic body.
- No organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
- 12. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply
- 13. Applies to leads number 1, 7, 8, and 14.
- 14. Lead configuration is optional within dimension BW except dimensions LW and LT apply.
- 15. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
- Pins 1, 7, 8, and 14 are collectors.
- 17. Pins 2, 6, 9, and 13 are bases. 18. Pins 3, 5, 10, and 12 are emitters. 19. Pins 4 and 11 are no contacts.

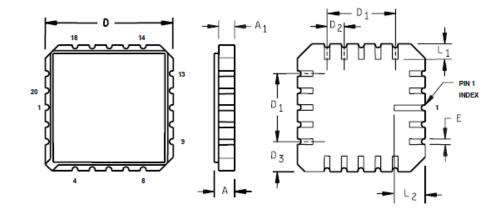
FIGURE 2. Physical dimensions for type 2N6988 - Continued.



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Outline Drawing 2N6987U



Symbol	Dimensions				
	Inches		Millimeters		
	Min	Max	Min	Max	
Α	.073	.085	1.85	2.16	
A ₁	.063	.075	1.60	1.90	
D	.345	.355	8.76	9.02	
D ₁	.195	.205	4.95	5.21	
D ₂	.050	ΙΥΡ	1.27 TYP		
D ₃	.070	.080	1.76	2.03	
E	.025 F	REF	0.64 F	REF	
L ₁	.050 REF		1.27 F	REF	
L ₂	.080	.090	2.03	2.28	

NOTES:

- 1. Dimensions are in inches.
- 2. Millimeters equivalents are given for general information only.
- 3. Unless otherwise specified, tolerance is ±.005 inch (0.13 mm).
- 4. For terminal connections, see figure 4.
- 5. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

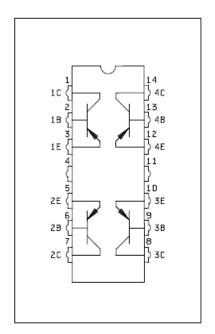
FIGURE 3. Physical dimensions for type 2N6987U.



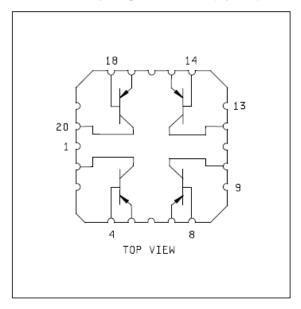
Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

Outline Drawing



14-lead flat-package or dual-in-line (top view)



20 pin leadless chip carrier (top view).

FIGURE 4. Schematic and terminal connections.



Multiple (Quad) PNP Silicon Dual In-Line And Flatpack Switching Transistor

Rev. V2

VPT COMPONENTS. ALL RIGHTS RESERVED.

Information in this document is provided in connection with VPT Components products. These materials are provided by VPT Components as a service to its customers and may be used for informational purposes only. Except as provided in VPT Components Terms and Conditions of Sale for such products or in any separate agreement related to this document, VPT Components assumes no liability whatsoever. VPT Components assumes no responsibility for errors or omissions in these materials. VPT Components may make changes to specifications and product descriptions at any time, without notice. VPT Components makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions. No license, express or implied, by estoppels or otherwise, to any intellectual property rights is granted by this document.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF VPT COMPONENTS PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. VPT COMPONENTS FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CON-TAINED WITHIN THESE MATERIALS. VPT COMPONENTS SHALL NOT BE LIABLE FOR ANY SPECIAL, IN-DIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVE-NUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

VPT Components products are not intended for use in medical, lifesaving or life sustaining applications. VPT Components customers using or selling VPT Components products for use in such applications do so at their own risk and agree to fully indemnify VPT Components for any damages resulting from such improper use or sale.