



2N70-CB

Preliminary

Power MOSFET

2A, 700V N-CHANNEL POWER MOSFET

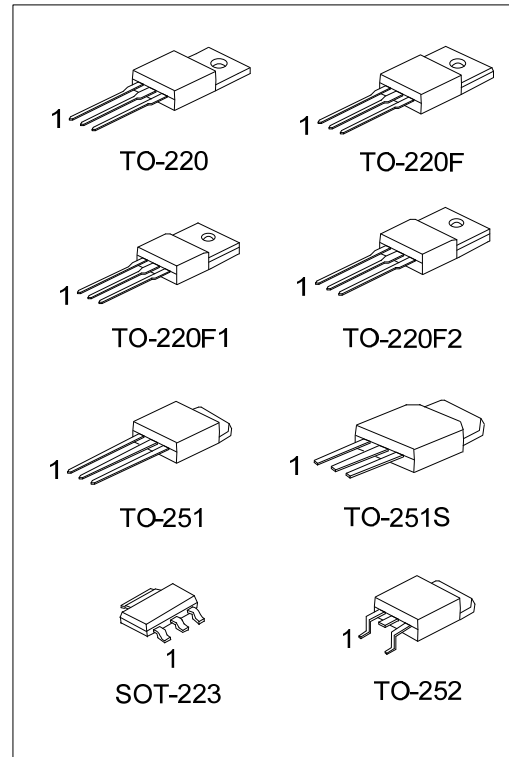
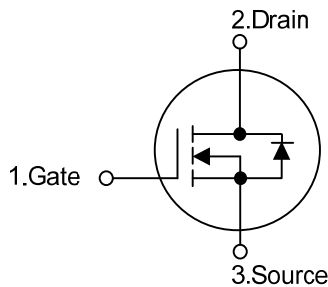
DESCRIPTION

The UTC **2N70-CB** is a high voltage MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} < 6.0\Omega @ V_{GS} = 10V, I_D = 1.0 A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



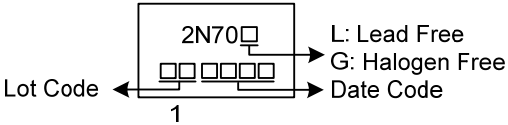
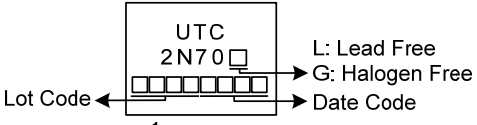
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N70L-AA3-R	2N70G-AA3-R	SOT-223	G	D	S	Tape Reel
2N70L-TA3-T	2N70G-TA3-T	TO-220	G	D	S	Tube
2N70L-TF1-T	2N70G-TF1-T	TO-220F1	G	D	S	Tube
2N70L-TF1-T	2N70G-TF1-T	TO-220F1	G	D	S	Tube
2N70L-TF3-T	2N70G-TF3-T	TO-220F	G	D	S	Tube
2N70L-TM3-T	2N70G-TM3-T	TO-251	G	D	S	Tube
2N70L-TMS-T	2N70G-TMS-T	TO-251S	G	D	S	Tube
2N70L-TN3-R	2N70G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2N70G-AA3-R</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) AA3: SOT-223, TA3: TO-220, TF3: TO-220F, TF1: TO-220F1, TF2: TO-220F2, TM3: TO-251, TMS: TO-251S, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

SOT-223	TO-220 / TO-220F / TO-220F1 / TO-220F2 TO-251 / TO-251S / TO-252
 <p>The diagram shows a SOT-223 package with the marking '2N70' and a small square symbol. Below the marking are four small squares representing a date code. An arrow points from the date code to the text 'Date Code'. To the left, an arrow points from the package to the text 'Lot Code'. Below the package is the number '1'. To the right of the package, an arrow points to the text 'L: Lead Free', another arrow points to 'G: Halogen Free', and a third arrow points to 'Date Code'.</p>	 <p>The diagram shows a TO-220/TO-251 package with the marking 'UTC' and '2N70' and a small square symbol. Below the marking are six small squares representing a date code. An arrow points from the date code to the text 'Date Code'. To the left, an arrow points from the package to the text 'Lot Code'. Below the package is the number '1'. To the right of the package, an arrow points to the text 'L: Lead Free', another arrow points to 'G: Halogen Free', and a third arrow points to 'Date Code'.</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	700	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	2.0	A
	Pulsed (Note 2)	I_{DM}	8.0	A
Avalanche Current (Note 2)		I_{AR}	2.4	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	29	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.75	V/ns
Power Dissipation	SOT-223	P_D		W
	TO-220		45	W
	TO-220F/TO-220F1 TO-220F2		28	W
	TO-251/TO-251S TO-252		30	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=10\text{mH}$, $I_{AS}=2.4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 2.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient	SOT-223	θ_{JA}		$^\circ\text{C}/\text{W}$
	TO-220/TO-220F TO-220F1/TO-220F2		62.5	$^\circ\text{C}/\text{W}$
	TO-251/TO-251S TO-252		110	$^\circ\text{C}/\text{W}$
Junction to Case	SOT-223	θ_{JC}		$^\circ\text{C}/\text{W}$
	TO-220		2.78	$^\circ\text{C}/\text{W}$
	TO-220F/TO-220F1 TO-220F2		4.46	$^\circ\text{C}/\text{W}$
	TO-251/TO-251S TO-252		4.17	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	700			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 700V, V_{GS} = 0V$			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
	Reverse					
		$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 1.0A$			6.0	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		295		pF
Output Capacitance	C_{OSS}			31		pF
Reverse Transfer Capacitance	C_{RSS}			5		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS} = 50V, V_{GS} = 10V, I_D = 1.3A$ $I_G = 100\mu A$ (Note 1, 2)		28		nC
Gate to Source Charge	Q_{GS}			1.6		nC
Gate to Drain Charge	Q_{GD}			1.4		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS} = 30V, V_{GS} = 10V, I_D = 0.5A,$ $R_G = 25\Omega$ (Note 1, 2)		36		ns
Rise Time	t_R			24		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			86		ns
Fall-Time	t_F			27		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Pulsed Current	I_{SD}				2.0	A
Drain-Source Diode Forward Voltage (Note 1)	I_{SM}				8.0	A
Maximum Body-Diode Continuous Current	V_{SD}	$V_{GS} = 0V, I_{SD} = 2.0A$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$V_{GS} = 0V, I_S = 2.0A,$ $dI_F / dt = 100A/\mu s$		315		nS
Body Diode Reverse Recovery Charge	Q_{rr}			0.8		μC

- Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

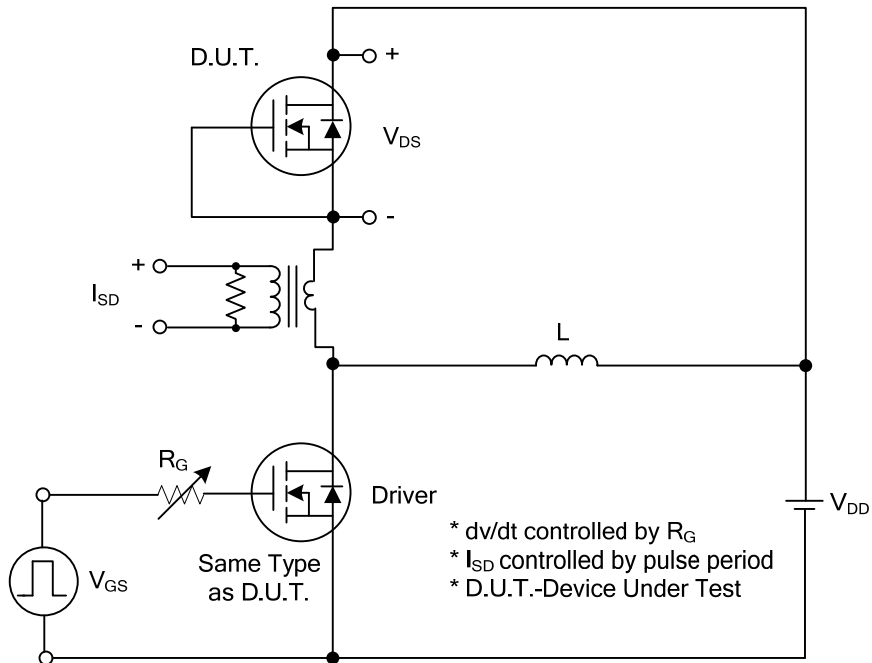


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

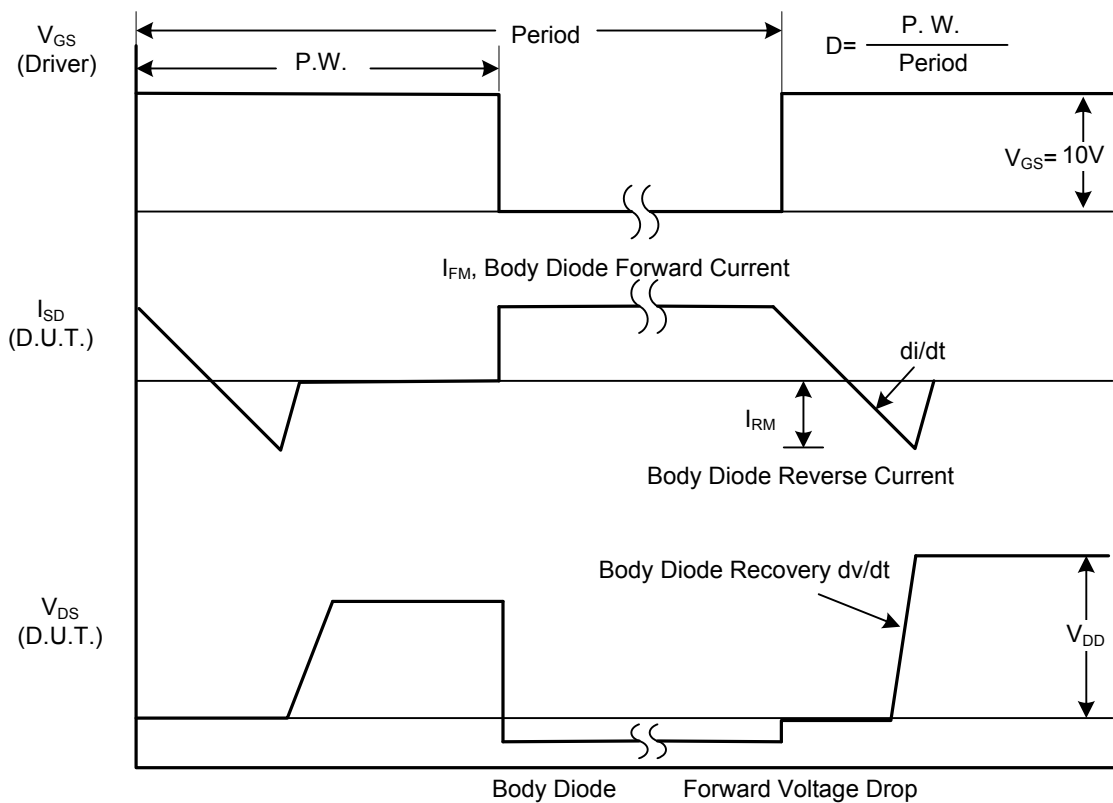


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

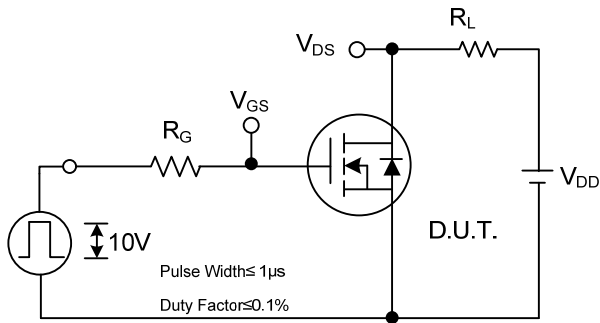


Fig. 2A Switching Test Circuit

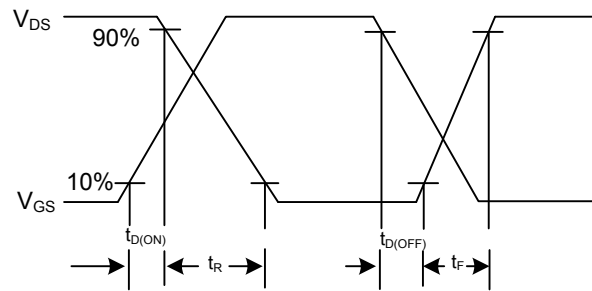


Fig. 2B Switching Waveforms

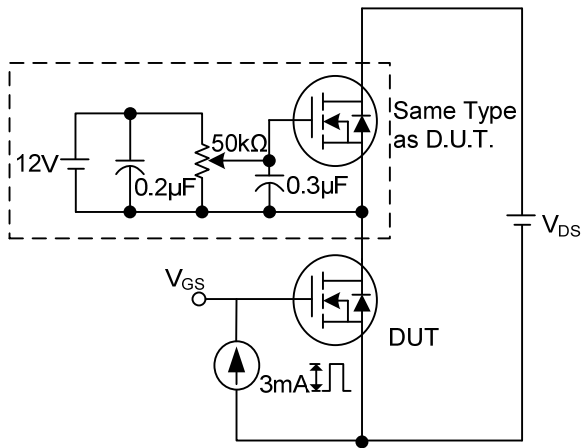


Fig. 3A Gate Charge Test Circuit

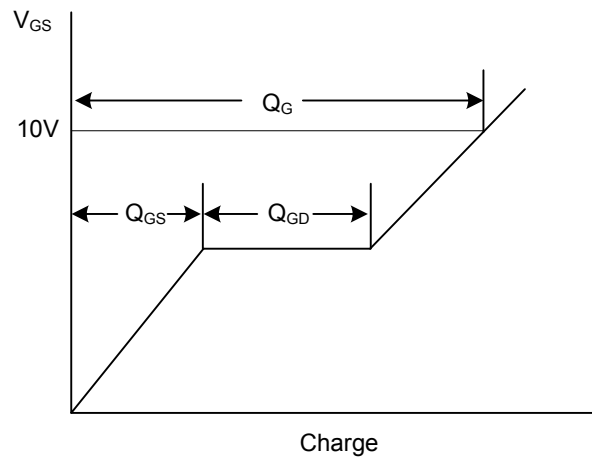


Fig. 3B Gate Charge Waveform

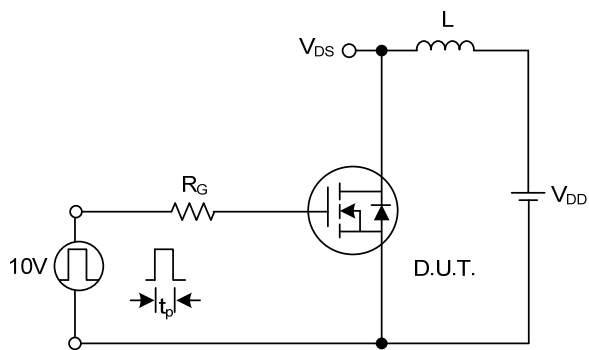


Fig. 4A Unclamped Inductive Switching Test Circuit

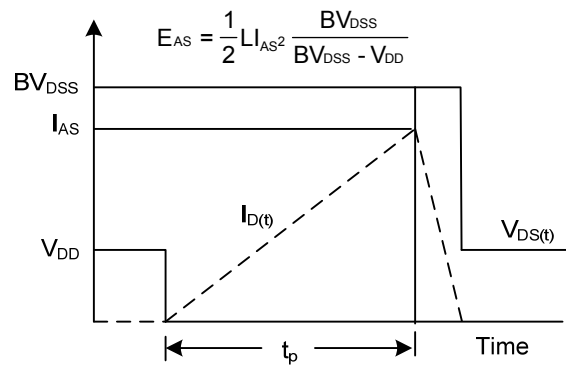


Fig. 4B Unclamped Inductive Switching Waveforms

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