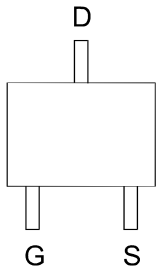
N-Channel MOSFET – ESD Protected

Features:

- Simple Drive Requirement
- Small Package Outline
- ROHS Compliant
- ESD Rating = 2000V HBM

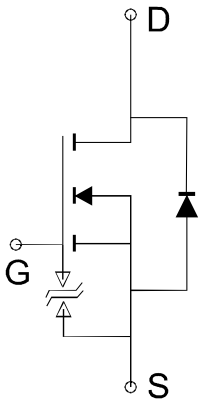
(SOT-23)

Top View



Applications:

- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switching.
- Rugged and reliable.
- High saturation current capability.
- High-speed switching.
- Not thermal runaway.
- The soldering temperature and time shall not exceed 260℃ for more than 10 seconds.



GENERAL DESCRIPTION

The 2N7002D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	300	mA
Pulsed Drain Current (Note 1)	I_{DM}	2000	mA
Maximum Power Dissipation	P_D @T_A=25?C	0.35	W
	P_D @T_A=75?C	0.21	
Operating Junction and Storage Temperature Range	T_J, Tstg	-55 ~ 150	℃
Junction-to-Ambient Thermal Resistance (PCB mounted) (Note 2)	$R_{\theta JA}$	357	℃/W

Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0, I_D=10uA	60	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.0	-	2.5	V
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D=250mA	100	-	-	mS
I_{GSS}	Gate Body Leakage	V_{GS}=±20V , V_{DS}=0V	-	-	±10	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V	-	-	1	uA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=500mA	-	-	3	Ω
		V_{GS}=4.5V, I_D=200mA	-	-	4	
		V_{GS}=3V, I_D=10mA	-	-	4.5	
Dynamic						
Q_g	Total Gate Charge	I_D=200mA , V_{DS}=15V V_{GS}=4.5V	-	-	0.8	nC
$T_{d(on)}$	Turn-on Time	V_{DD}=30V , R_L=150Ω, I_D=200mA , V_{GEN}=10V R_G=10Ω	-	-	20	nS
$T_{d(off)}$	Turn-off Time		-	-	40	
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	-	-	35	pF
C_{oss}	Output Capacitance		-	-	10	
C_{rss}	Reverse Transfer Capacitance		-	-	5	

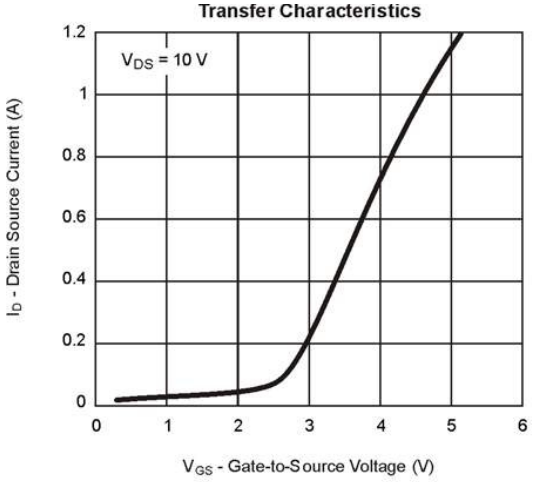
Source-Drain Diode

Symbol	Parameter	Limit	Min.	Typ.	Max.	Unit
V_{SD}	Diode Forward Voltage	I_S=200mA, V_{GS}=0V	-	0.82	1.3	V

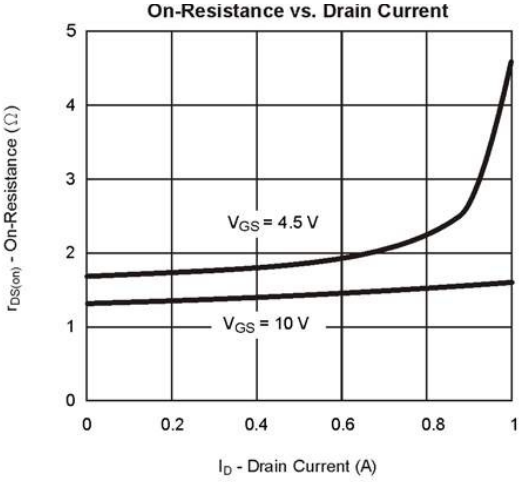
Notes : 1.Maximum DC current imited by the package.

2.Surface mounted on Fr4 board, t ≦ 5sec.

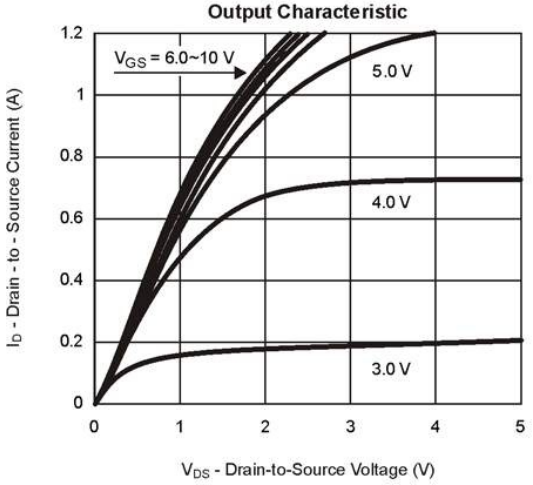
Transfer Characteristics



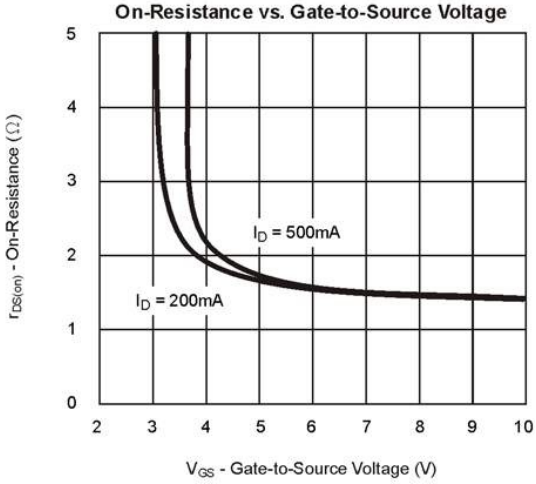
On-Resistance vs. Drain Current



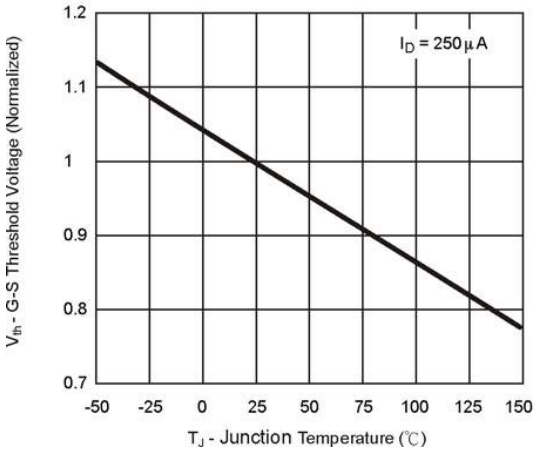
Output Characteristic



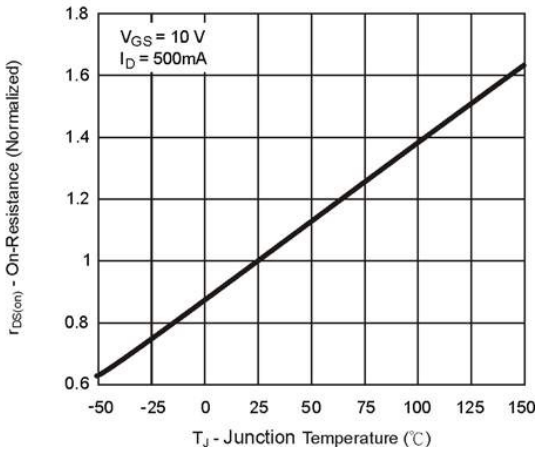
On-Resistance vs. Gate-to-Source Voltage



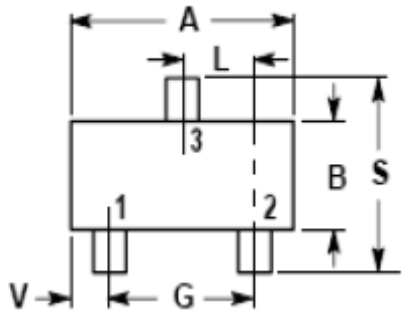
Threshold Voltage vs. Temperature

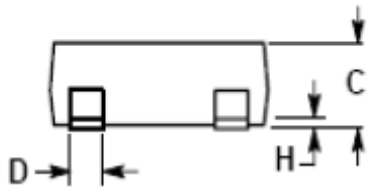


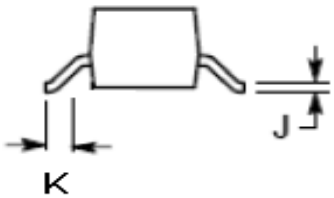
On-Resistance vs. Junction Temperature



SOT-23 Package Outline



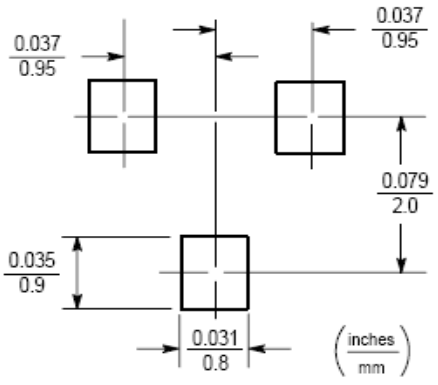




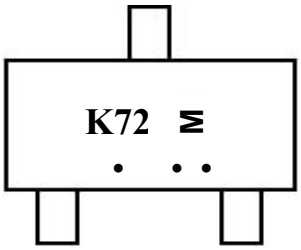
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.5
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.007	-	0.018	-
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

SOLDERING FOOTPRINT*



Device name:2N7002D
Package:SOT-23
Marking Code:



K72: Device Marking Code
M: Date code

MONTH CODE

ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z

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