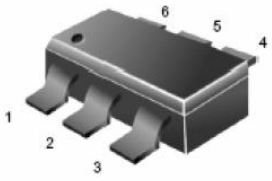
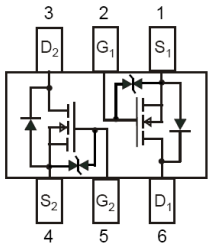
Main Product Characteristics:

V_{DSS}	60V
R_{DS}(on)	7.5ohm(max.)
I_D	A



SOT-363



Schematic diagram

Features and Benefits:

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150℃ operating temperature

Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute max Rating:

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	60	V
Gate-Source Voltage	VGS	±20	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I_D	0.115	A
	I_{DM}	0.8	A
Maximum Power Dissipation	P_D	0.38	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

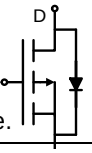
Thermal Resistance

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	328	℃/W

Electrical Characterizes @T_A=25℃ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±1	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1		2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.5A			7.5	Ω
		V_{GS}=5V, I_D=0.05A			7.5	
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=0.2A	0.08			S
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz		30		PF
Output Capacitance	C_{oss}			6		PF
Reverse Transfer Capacitance	C_{rss}			3		PF
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, ID=0.2A, V_{GS}=10V,R_{GEN}=10Ω			20	nS
Turn-Off Delay Time	$t_{d(off)}$				40	nS

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.115	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	0.8	A	
V_{sd}	Diode Forward Voltage	—	—	1.3	V	I_S=0.2A, V_{GS}=0V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

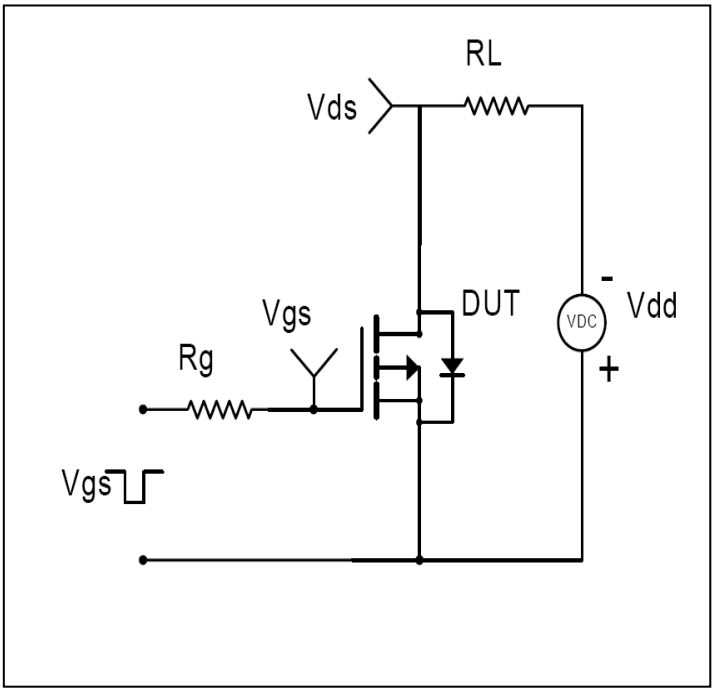


Figure 1: **Switching Test Circuit**

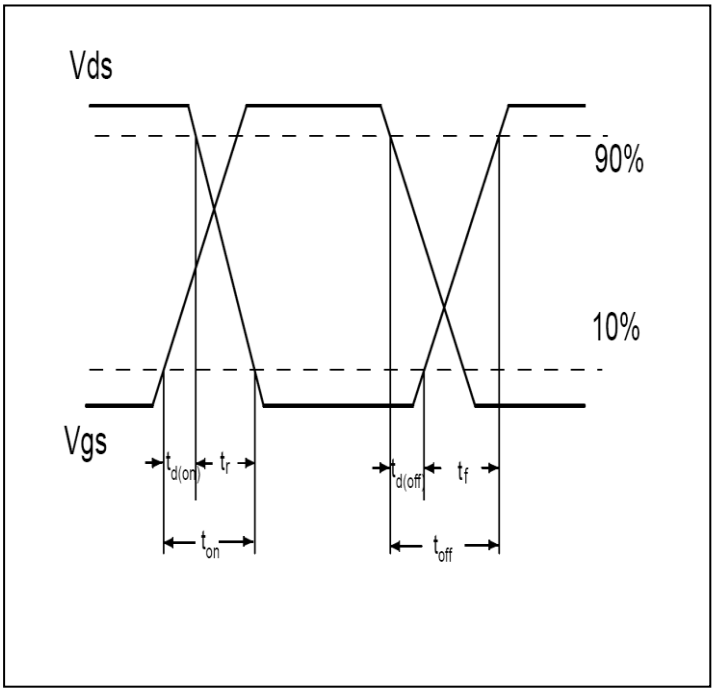


Figure 2: **Switching Waveforms**

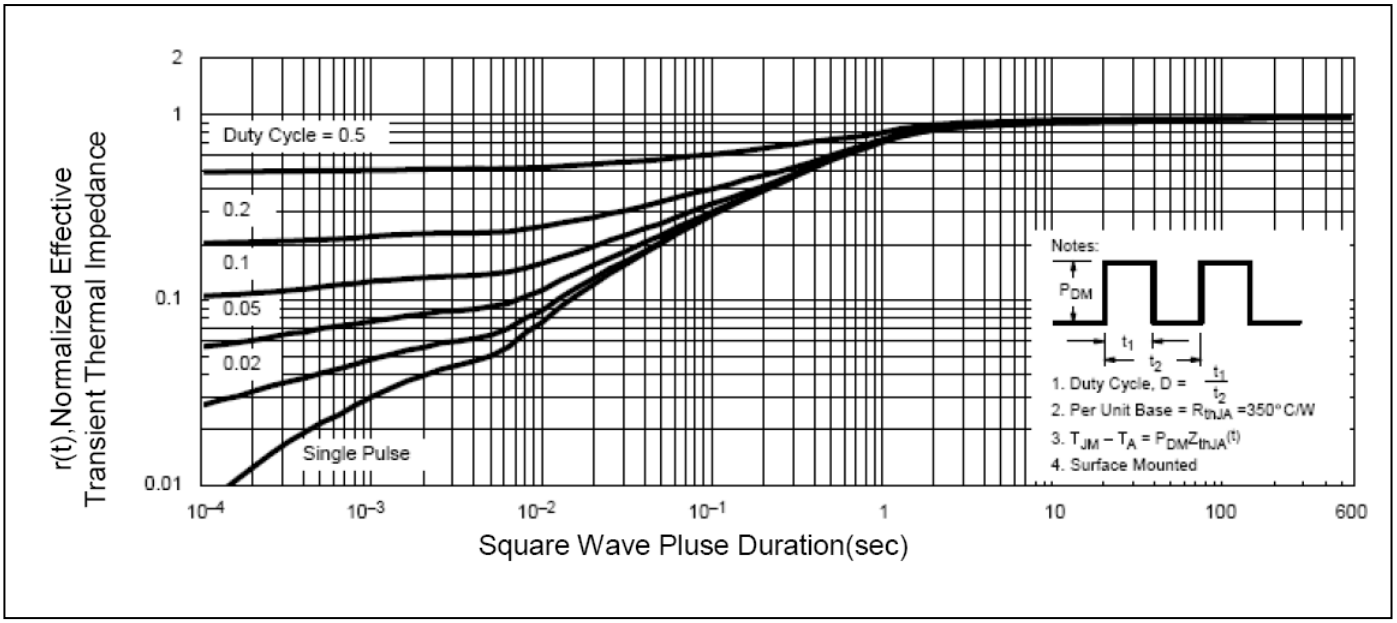
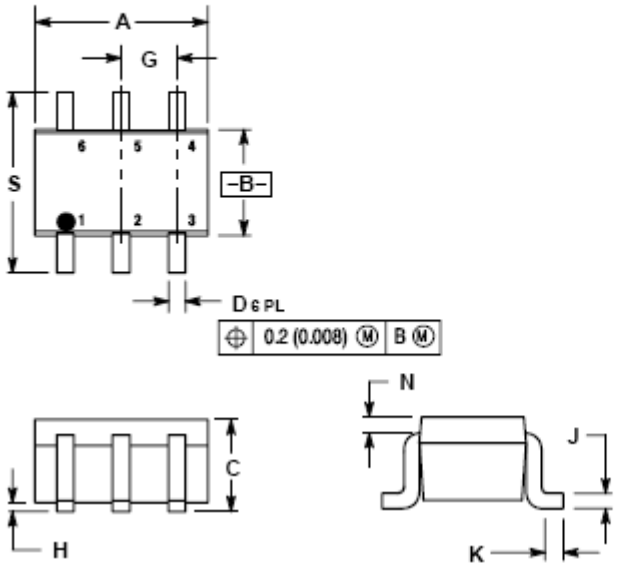


Figure3. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data：

SC−88 (SOT−363)
CASE 419B−02
ISSUE T

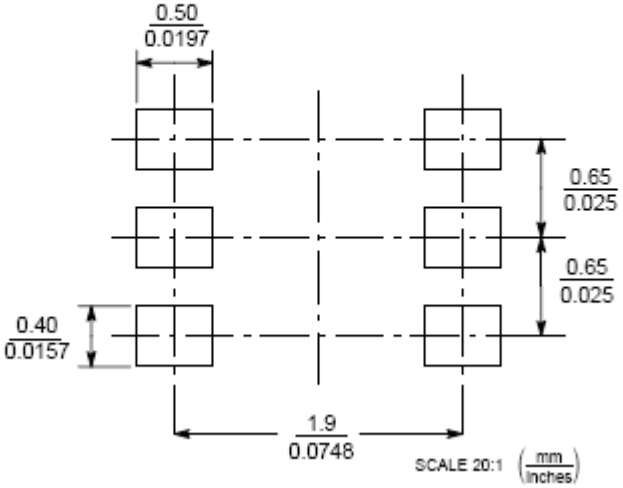


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

SOLDERING FOOTPRINT*



NOTES：

1. Dimensions are inclusive of plating
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter; converted inch dimensions are not necessarily exact.

Ordering and Marking Information

Device Marking: 702

Package (Available)
SOT-363
Operating Temperature Range
C : -55 to 150 ºC

Devices per Unit

Package Type	Units/ Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
SOT-363	3000	10	30000	4	120000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃ or 150℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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