October 2014

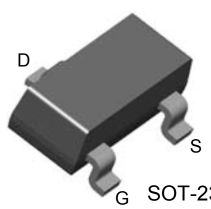
2N7002L
N-Channel Enhancement Mode Field Effect Transistor

Features

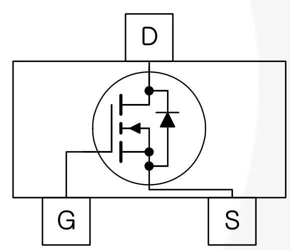
- High Density Cell Design for Low $R_{DS(ON)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable
- High Saturation Current Capability
- Very Low Capacitance
- Fast Switching Speed

Description

This N-channel enhancement mode field effect transistor is produced using high cell density, trench MOSFET technology. This product minimizes on-state resistance while providing rugged, reliable and fast switching performance. This product is particularly suited for low-voltage, low-current applications such as small servo motor control, power MOSFET gate drivers, logic level translator, high speed line drivers, power management/power supply, and switching applications.



SOT-23



Ordering Information

Part Number	Marking	Package	Packing Method
2N7002L	70L	SOT-23 3L	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-Source Voltage		60	V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)		60	V
V_{GSS}	Gate-Source Voltage	Continuous	±20	V
		Non Repetitive (t_p < 50 µs)	±40	
I_D	Maximum Drain Current	Continuous	115	mA
		Pulsed	800	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16 inch from Case for 10 Seconds		300	°C

Thermal Characteristics[1]

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Maximum Power Dissipation	200	mW
	Derate Above 25°C	1.6	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	380	°C/W

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 380°C/W when mounted on a minimum pad.

Scale 1: 1 on letter size paper

ESD Rating[2]

Symbol	Parameter	Value	Unit
HBM	Human Body Model per ANSI/ESDA/JEDEC JS-001-2012	50	V
CDM	Charged Device Model per JEDEC C101C	>2000	V

Note:

2. ESD values are in typical, no over-voltage rating is implied, ESD CDM zap voltage is 2000 V maximum.

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 µA	60.0	65.2		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V		0.024	1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125°C		0.080	500	
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V		0.107	100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V		-0.037	-100	nA
On Characteristics(3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.80	1.81	2.50	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 500 mA		3.35	7.50	Ω
		V_{GS} = 10 V, I_D = 500 mA, T_J = 100°C		5.62	13.50	
		V_{GS} = 5 V, I_D = 50 mA		2.68	7.50	
		V_{GS} = 5 V, I_D = 50 mA, T_J = 100°C		3.97	13.50	
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS} = 10 V, I_D = 500 mA		1.68	3.75	V
		V_{GS} = 5 V, I_D = 50 mA		0.13	1.50	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} ≥ 2 $V_{DS(ON)}$	500	557		mA
		V_{GS} = 4.5 V, V_{DS} = 10 V	75	571		
g_{FS}	Forward Trans-conductance	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 200 mA	80	214		mS
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		12.8	50	pF
C_{oss}	Output Capacitance			3.25	25	pF
C_{rss}	Reverse Transfer Capacitance			1.52	5	pF
R_G	Gate Resistance	V_{GS} = 0 V, f = 1.0 MHz		22.2		Ω
Switching Characteristics(3)						
t_{on}	Turn-On Time	V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω		4.35	20	ns
t_{off}	Turn-Off Time			15.6	20	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				115	mA
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				0.8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 115 mA(3)		0.818	1.5	V

Note:

3. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2.0%.

Typical Performance Characteristics

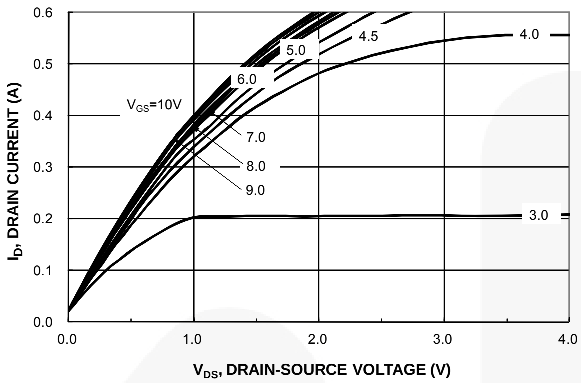


Figure 1. On-Region Characteristics

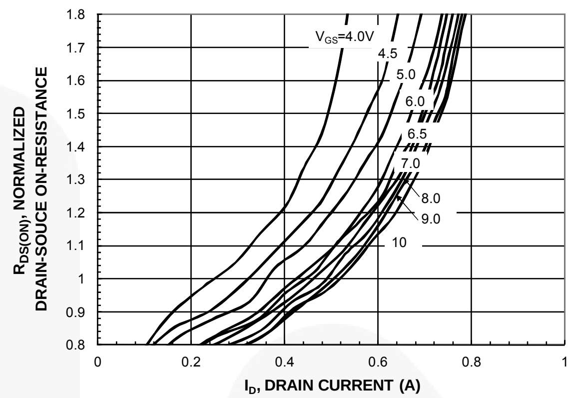


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

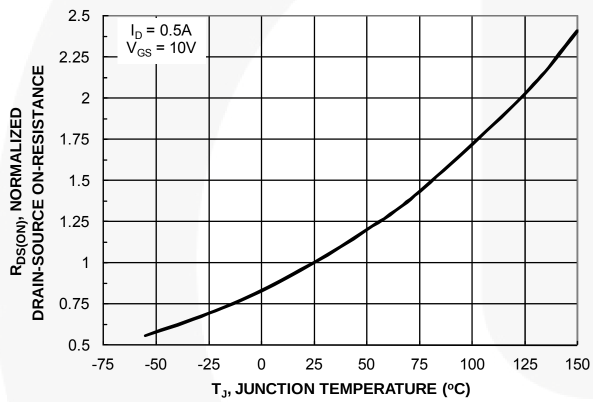


Figure 3. On-Resistance Variation with Temperature

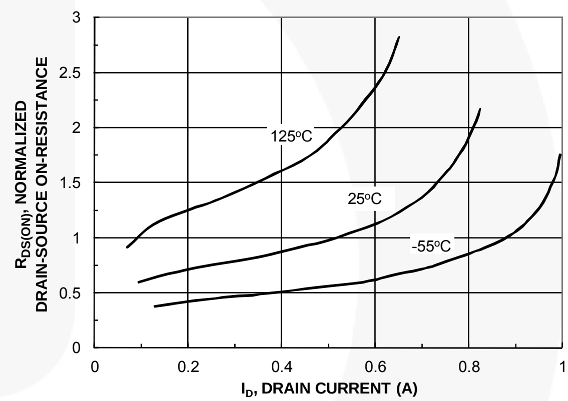


Figure 4. On-Resistance Variation with Drain Current and Temperature

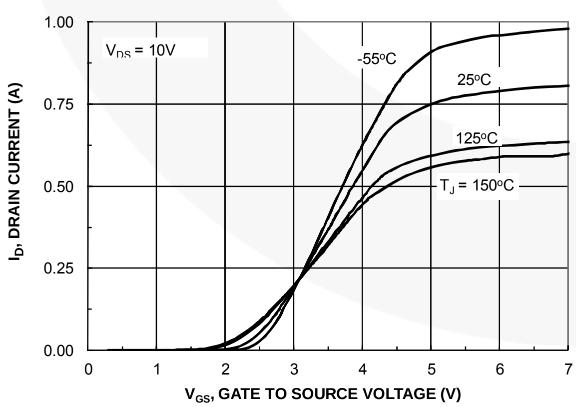


Figure 5. Transfer Characteristics

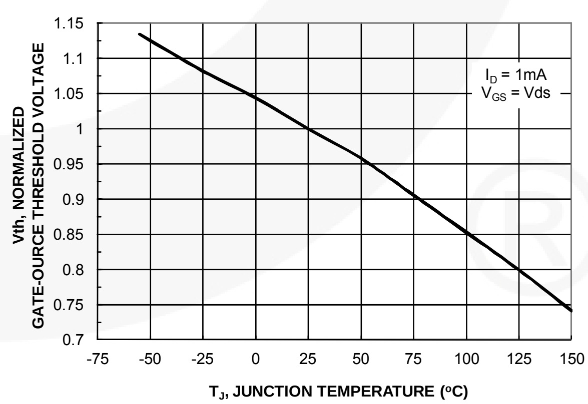


Figure 6. Gate Threshold Variation with Temperature

Typical Performance Characteristics (Continued)

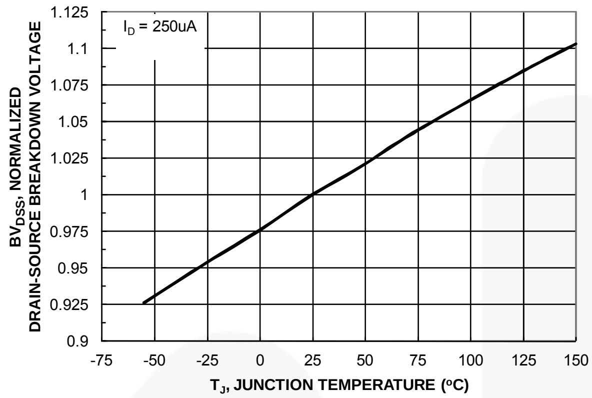


Figure 7. Breakdown Voltage Variation with Temperature

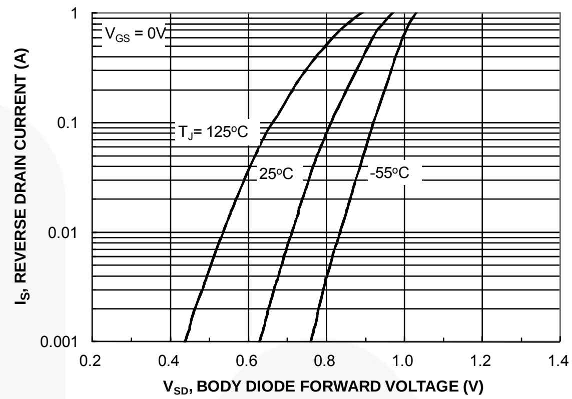


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

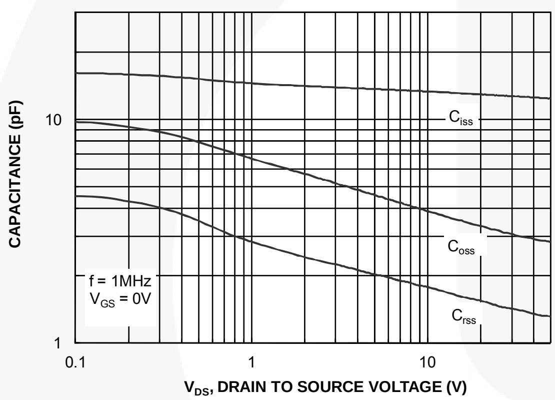


Figure 9. Capacitance Characteristics

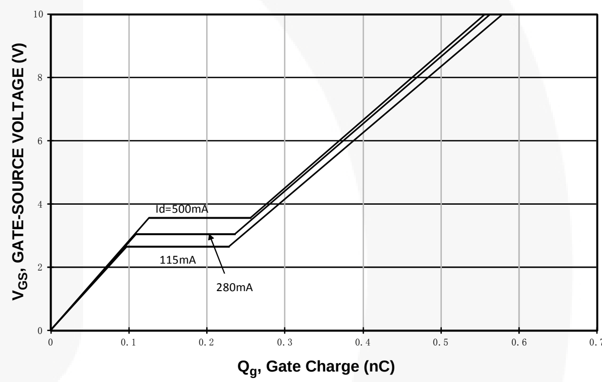


Figure 10. Gate Charge Characteristics

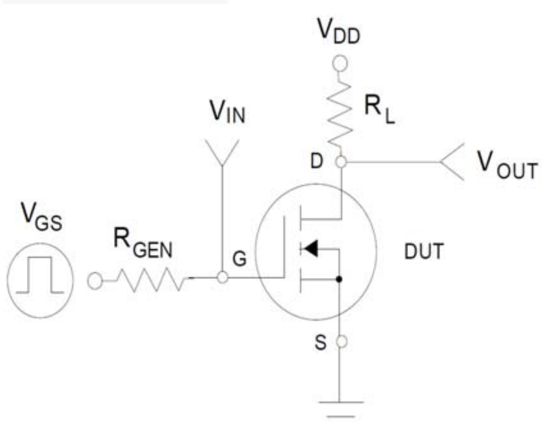


Figure 11.

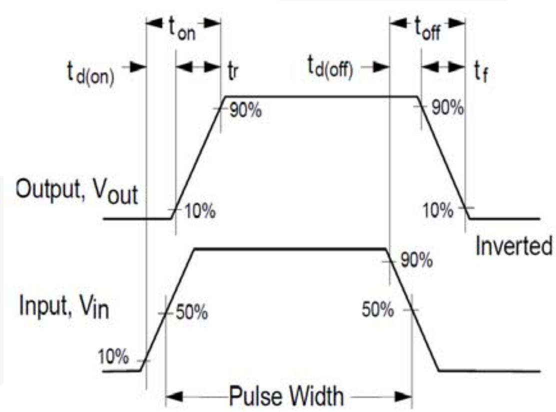


Figure 12. Switching Waveforms

Typical Performance Characteristics (Continued)

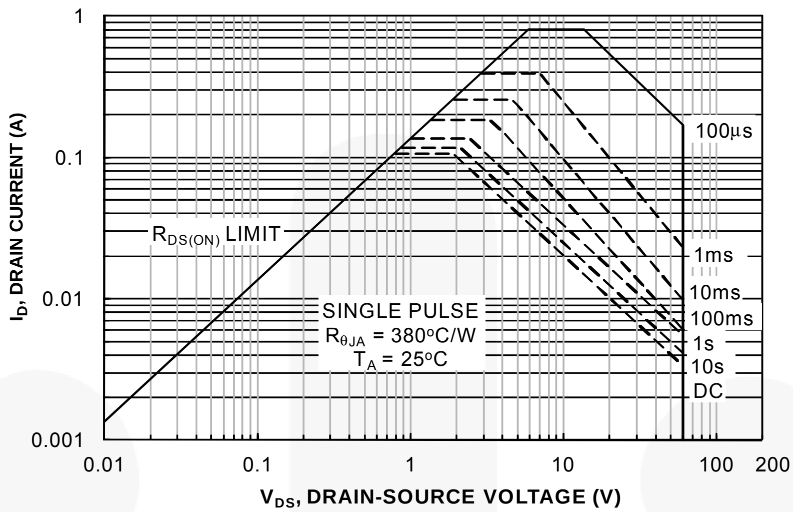


Figure 13. Maximum Safe Operating Area

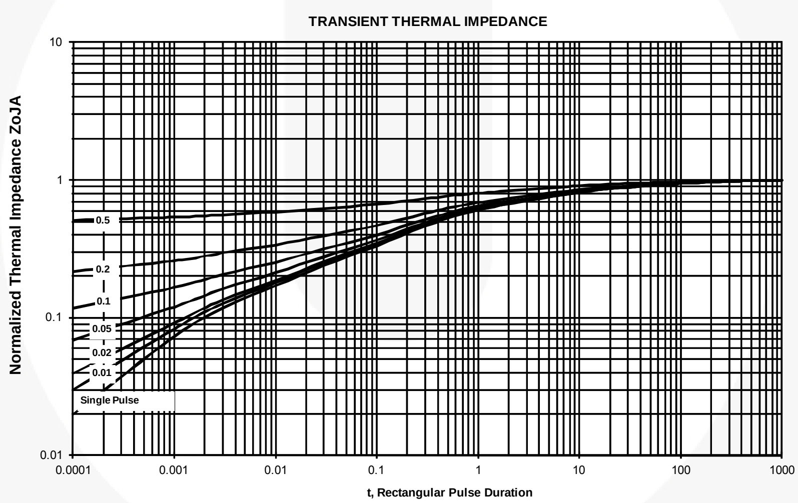
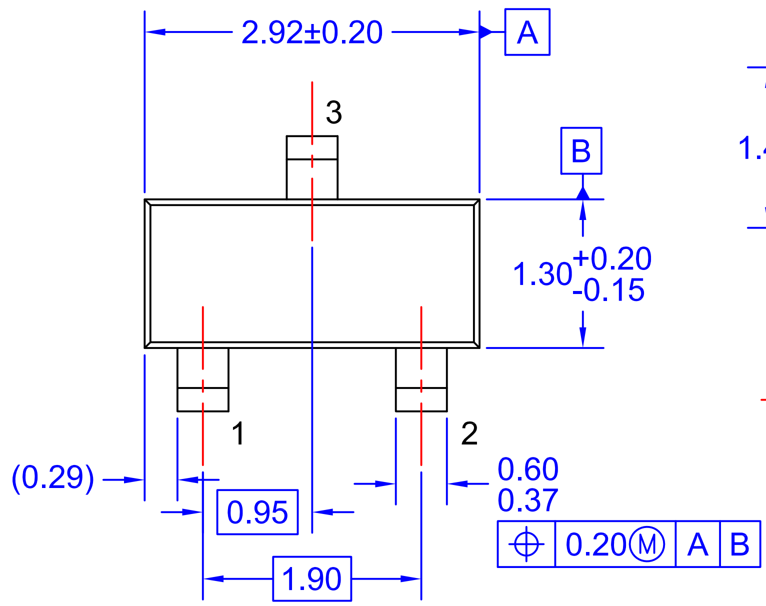
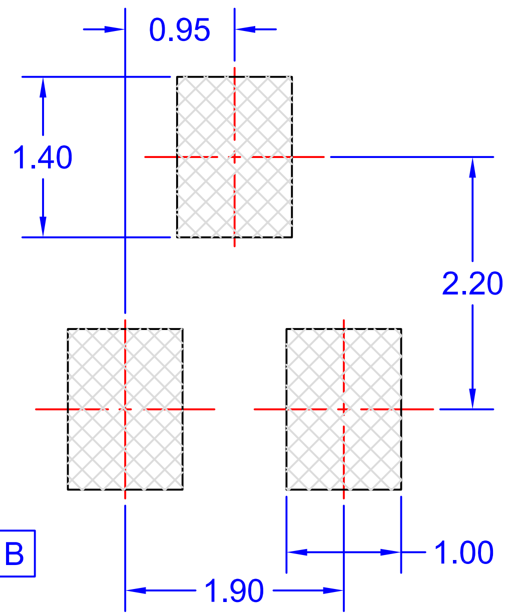
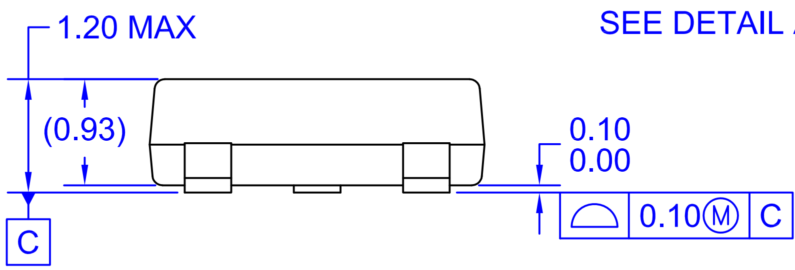


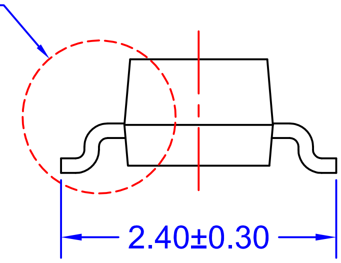
Figure 14. Transient Thermal Response Curve

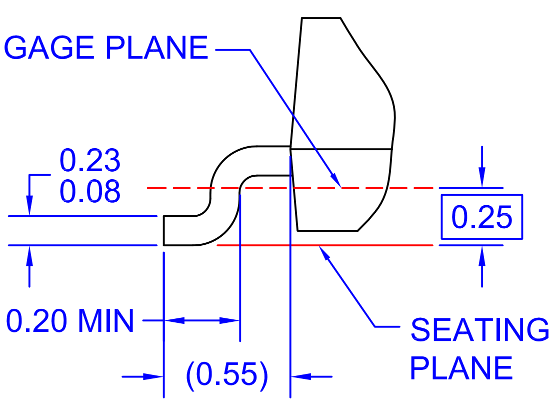




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
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C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
E) DRAWING FILE NAME: MA03DREV12

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