

RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

N-Channel SOT-323

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V _{DGR}	60	Vdc
Drain Current – Continuous $T_C = 25^\circ\text{C}$ (Note 1.) $T_C = 100^\circ\text{C}$ (Note 1.) – Pulsed (Note 2.)	I _D I _D I _{DM}	± 115 ± 75 ± 800	mAdc
Gate-Source Voltage – Continuous – Non-repetitive ($t_p \leq 50 \mu\text{s}$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk

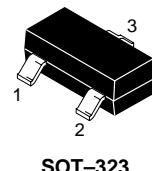
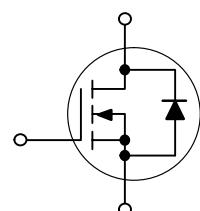
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 3.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P _D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	R _{θJA}	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate,(Note 4.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P _D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	R _{θJA}	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T _J , T _{stg}	-55 to +150	$^\circ\text{C}$

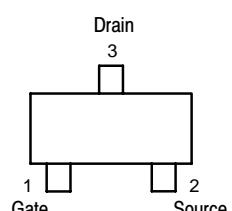
1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
3. FR-5 = $1.0 \times 0.75 \times 0.062$ in.
4. Alumina = $0.4 \times 0.3 \times 0.025$ in 99.5% alumina.

SOT-323		
Dim	Min	Max
A	1.800	2.200
B	1.150	1.350
C	0.800	1.000
D	0.300	0.400
G	1.200	1.400
H	0.000	0.100
J	0.100	0.250
K	0.350	0.500
L	0.590	0.720
S	2.000	2.400
V	0.280	0.420
All Dimension in mm		

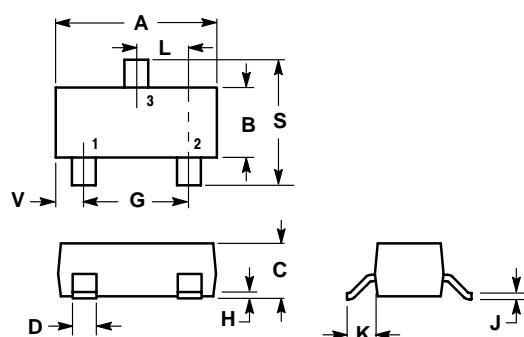
N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



K72 , 702 = Device Code



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain–Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 10 \mu\text{A}$)	$V_{(\text{BR})\text{DSS}}$	60	–	–	Vdc
Zero Gate Voltage Drain Current ($V_{GS} = 0$, $V_{DS} = 60 \text{ Vdc}$)	I_{DSS}	–	–	1.0 500	μA
Gate–Body Leakage Current, Forward ($V_{GS} = 20 \text{ Vdc}$)	I_{GSSF}	–	–	100	nAdc
Gate–Body Leakage Current, Reverse ($V_{GS} = -20 \text{ Vdc}$)	I_{GSSR}	–	–	-100	nAdc

ON CHARACTERISTICS (Note 2.)

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$)	$V_{GS(\text{th})}$	1.0	–	2.5	Vdc
On–State Drain Current ($V_{DS} \geq 2.0 \text{ V}$, $V_{DS(\text{on})}, V_{GS} = 10 \text{ Vdc}$)	$I_{\text{D(on)}}$	500	–	–	mA
Static Drain–Source On–State Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 500 \text{ mA}$) ($V_{GS} = 5.0 \text{ Vdc}$, $I_D = 50 \text{ mA}$)	$V_{DS(\text{on})}$	– –	– –	3.75 0.375	Vdc
Static Drain–Source On–State Resistance ($V_{GS} = 10 \text{ V}$, $I_D = 500 \text{ mA}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$ ($V_{GS} = 5.0 \text{ Vdc}$, $I_D = 50 \text{ mA}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	$r_{DS(\text{on})}$	– – – –	– – – –	7.5 13.5 7.5 13.5	Ohms
Forward Transconductance ($V_{DS} \geq 2.0 \text{ V}$, $I_D = 200 \text{ mA}$)	g_{FS}	80	–	–	mmhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{iss}	–	–	50	pF
Output Capacitance ($V_{DS} = 25 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{oss}	–	–	25	pF
Reverse Transfer Capacitance ($V_{DS} = 25 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{rss}	–	–	5.0	pF

SWITCHING CHARACTERISTICS (Note 2.)

Turn–On Delay Time	$(V_{DD} = 25 \text{ Vdc}, I_D \approx 500 \text{ mA}, R_G = 25 \Omega, R_L = 50 \Omega, V_{\text{gen}} = 10 \text{ V})$	$t_{\text{d(on)}}$	–	–	20	ns
Turn–Off Delay Time		$t_{\text{d(off)}}$	–	–	40	ns

BODY–DRAIN DIODE RATINGS

Diode Forward On–Voltage ($I_S = 11.5 \text{ mA}$, $V_{GS} = 0 \text{ V}$)	V_{SD}	–	–	-1.5	Vdc
Source Current Continuous (Body Diode)	I_S	–	–	-115	mAdc
Source Current Pulsed	I_{SM}	–	–	-800	mAdc

2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

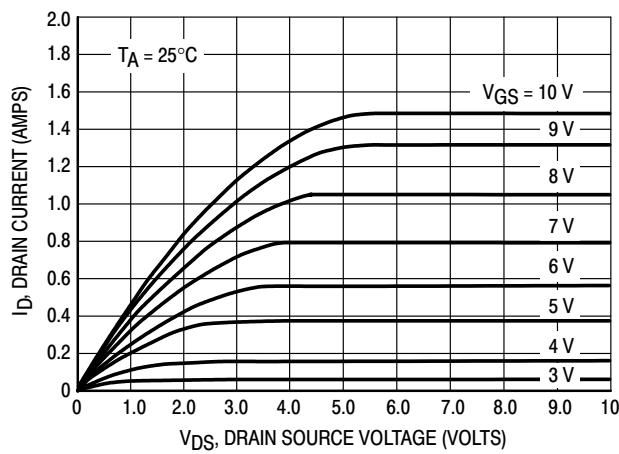


Figure 1. Ohmic Region

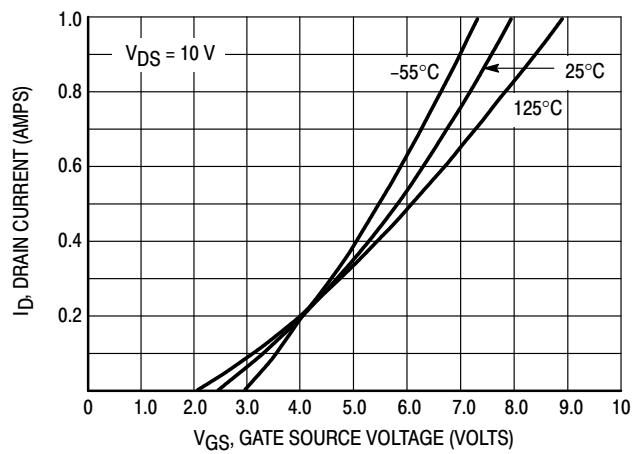


Figure 2. Transfer Characteristics

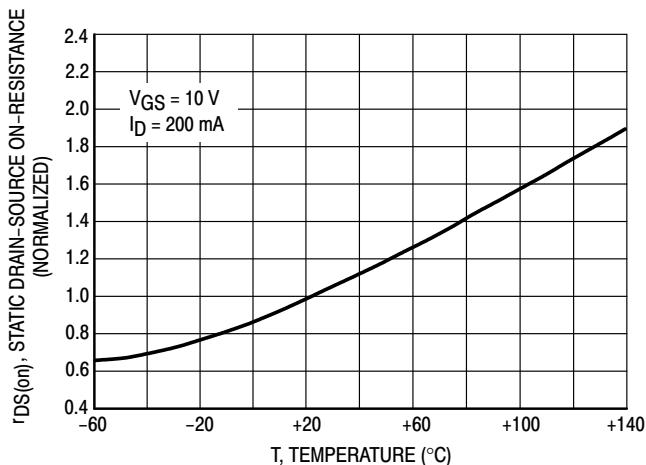


Figure 3. Temperature versus Static Drain-Source On-Resistance

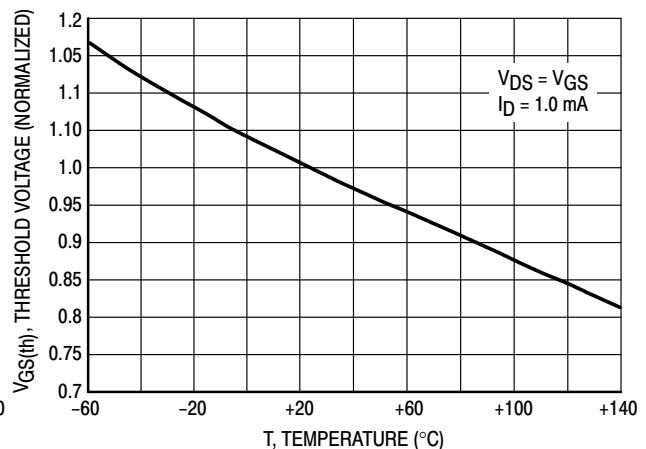


Figure 4. Temperature versus Gate Threshold Voltage