2N7105 SERIES

Siliconix incorporated

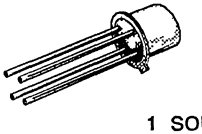
N-Channel Lateral DMOS FETs

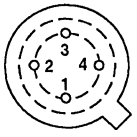
The 2N7105 Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. This series also feature an integrated Zener diode designed to protect the gate from electrical "spikes" or overstress.

For additional design information please see performance curves DMCB, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
2N7105	10	70	0.5	2
2N7107	10	70	0.5	2
2N7109	20	70	0.5	2

TO-72 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

SIMILAR PRODUCTS

- Quad Array, See 2N7116 Series
- SO-14 Array, See SD5400 Series
- SOT-143, See SST211 Series
- Chips, Order 2N710XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		2N7105	2N7107	2N7109	
Gate-Source, Gate-Drain Voltage	V_{GS},V_{GD}	-30/25	-15/25	-25/30	V
Gate-Substrate Voltage [1]	V_{GB}	-0.3/25	-0.3/25	-0.3/30	
Drain-Source Voltage	V_{DS}	30	10	20	
Source-Drain Voltage	V_{SD}	10	10	20	
Drain-Substrate Voltage	V_{DB}	30	15	25	
Source-Substrate Voltage	V_{SB}	15	15	25	
Drain Current	I_D	50	50	50	mA
Power Dissipation (T_J = 25°C)	P_D	300	300	300	mW
Power Derating		2.4	2.4	2.4	mW/°C
Operating Junction Temperature	T_J	-55 to 150			°C
Storage Temperature	T_{stg}	-65 to 200			
Lead Temperature (1/16" from case for 10 seconds)	T_L	300			

[1]These devices feature an internal Zener protected gate.

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N7105		2N7107		2N7109		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage[3]	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu A$		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage[3]	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage[3]	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source OPEN		35	15		15		25		
Source-Substrate Breakdown Voltage[3]	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu A$ Drain OPEN		35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
		$V_{GS} = V_{BS} = -5$ V, $T_A = 125°C$	$V_{DS} = 10$ V	0.4		5		5			µA
			$V_{DS} = 20$ V	0.9						5	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			nA
			$V_{SD} = 20$ V	1						10	
		$V_{GD} = -5$ V, $T_A = 125°C$	$V_{SD} = 10$ V	0.5		5		5			µA
			$V_{SD} = 20$ V	1						5	
Gate Leakage	I_{GSS}	$V_{DS} = V_{SB} = 0$ V	$V_{GS} = 25$ V			1		1			
			$V_{GS} = 30$ V							1	
		$V_{DS} = V_{SB} = 0$ V, $T_A = 125°C$	$V_{GS} = 25$ V			100		100			
			$V_{GS} = 30$ V							100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = V_{BS} = 0$ V				10					
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu A$, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 5$ V, $I_D = 1$ mA		58		70		70		70	Ω
DYNAMIC											
Forward Transconductance[3]	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz		11							mS
Output Conductance[3]	g_{os}			0.9							
Gate Node Capacitance	C_{iss}	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\ \Omega$, $V_{IN} = 5$ V, $R_G = 50\ \Omega$		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time [3]	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25°C$ unless otherwise noted.
2. For design aid only, not subject to production testing.
3. This parameter not registered with JEDEC.

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