

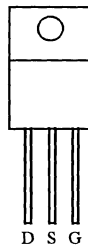
N-Channel Enhancement-Mode Transistors

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.105	27.4

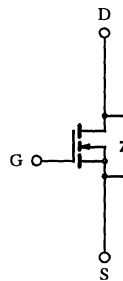
Parametric limits in accordance with MIL-S-19500/592 where applicable.

TO-254AA
Hermetic Package



Top View

Case Isolated



N-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	27.4
		$T_C = 100^\circ\text{C}$	17
Pulsed Drain Current	I_{DM}	110	A
Avalanche Current	I_{AR}	27.4	
Maximum Power Dissipation	P_D	150	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

6
N-/P-Channel
MOSFETS

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	0.83	$^\circ\text{C/W}$

2N7225JANTX/JANTXV

Siliconix

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ ^a	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1000\ \mu\text{A}$	200			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}, T_J = -55^\circ\text{C}$			5.0	
		$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}, T_J = 25^\circ\text{C}$	2.0		4.0	
		$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}, T_J = 125^\circ\text{C}$	1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}, T_J = 125^\circ\text{C}$			± 200	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}$			25	μA
		$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			250	
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			1000	
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 27.4\text{ A}$			0.105	Ω
		$V_{GS} = 10\text{ V}, I_D = 17\text{ A}, T_J = 125^\circ\text{C}$			0.17	
Dynamic						
Total Gate Charge ^c	Q_g	$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 27.5\text{ A}$	55		115	nC
Gate-Source Charge ^c	Q_{GS}		8		22	
Gate-Drain Charge ^c	Q_{GD}		30		60	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 100\text{ V}, R_L = 3.6\ \Omega$ $I_D \cong 27.4\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.35\ \Omega$			35	ns
Rise Time ^c	t_r				190	
Turn-Off Delay Time ^c	$t_{d(off)}$				170	
Fall Time ^c	t_f				130	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				27.4	A
Pulsed Current	I_{SM}				110	
Diode Forward Voltage ^b	V_{SD}	$I_F = 27.4\text{ A}, V_{GS} = 0\text{ V}$	0.8		1.9	V
Reverse Recovery Time	t_{rr}	$I_F = 27.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$			950	ns

Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Independent of operating temperature.