

**RADIATION HARDENED  
LOGIC LEVEL POWER MOSFET  
SURFACE MOUNT (LCC-6)**

**60V, DUAL N-CHANNEL  
R7 TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>
IRHLUC770Z4	100 kRads(Si)	0.75Ω	0.89A
IRHLUC730Z4	300 kRads(Si)	0.75Ω	0.89A



**Description**

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

**Features**

- 5V CMOS and TTL Compatible
- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Light Weight
- Surface Mount
- Complementary P-Channel Available - IRHLUC7970Z4
- ESD Rating: Class 0 per MIL-STD-750, Method 1020

**Absolute Maximum Ratings (Each N-Ch Die)**

**Pre-Irradiation**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = 4.5V, T <sub>C</sub> = 25°C	Continuous Drain Current	0.89	A
I <sub>D2</sub> @ V <sub>GS</sub> = 4.5V, T <sub>C</sub> = 100°C	Continuous Drain Current	0.56	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	3.56	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	1.0	W
	Linear Derating Factor	0.01	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 10	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	20	mJ
I <sub>AR</sub>	Avalanche Current ①	0.89	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	0.1	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.7	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temperature	300 (for 5s)	
	Weight	0.2 (Typical)	g

For Footnotes, refer to the page 2.

**Electrical Characteristics (Each N-Ch Die) @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.75	Ω	V <sub>GS</sub> = 4.5V, I <sub>D2</sub> = 0.56A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-4.5	—	mV/°C	
G <sub>fs</sub>	Forward Transconductance	1.1	—	—	S	V <sub>DS</sub> = 15V, I <sub>D2</sub> = 0.56A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	1.0	μA	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V
		—	—	10		V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 10V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -10V
Q <sub>G</sub>	Total Gate Charge	—	—	3.6	nC	I <sub>D1</sub> = 0.89A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	1.5		V <sub>DS</sub> = 30V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	1.8		V <sub>GS</sub> = 4.5V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	8.0	ns	V <sub>DD</sub> = 30V
t <sub>r</sub>	Rise Time	—	—	15		I <sub>D1</sub> = 0.89A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	30		R <sub>G</sub> = 24Ω
t <sub>f</sub>	Fall Time	—	—	12		V <sub>GS</sub> = 5.0V
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	33	—	nH	Measured from center of Drain pad to center of Source pad
C <sub>iSS</sub>	Input Capacitance	—	145	—	pF	V <sub>GS</sub> = 0V
C <sub>oSS</sub>	Output Capacitance	—	43	—		V <sub>DS</sub> = 25V
C <sub>rSS</sub>	Reverse Transfer Capacitance	—	2.5	—		f = 1.0MHz
R <sub>G</sub>	Gate Resistance	—	9.5	—	Ω	f = 1.0MHz, open drain

**Source-Drain Diode Ratings and Characteristics (Each N-Ch Die)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	0.89	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	3.56		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 0.89A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	65	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 0.89A, V <sub>DD</sub> ≤ 25V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	67	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Thermal Resistance (Each N-Ch Die)**

Symbol	Parameter	Min.	Typ.	Max.	Units
R <sub>θJA</sub>	Junction-to-Ambient	—	—	125	°C/W
R <sub>θJL</sub>	Junction-to-Lead	—	—	40	

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 50.4mH, Peak I<sub>L</sub> = 0.89A, V<sub>GS</sub> = 10V
- ③ I<sub>SD</sub> ≤ 0.89A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ 60V, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V<sub>GS</sub> Bias. 10 volt V<sub>GS</sub> applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V<sub>DS</sub> Bias. 48 volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

## Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table1. Electrical Characteristics (Each N-Ch Die) @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

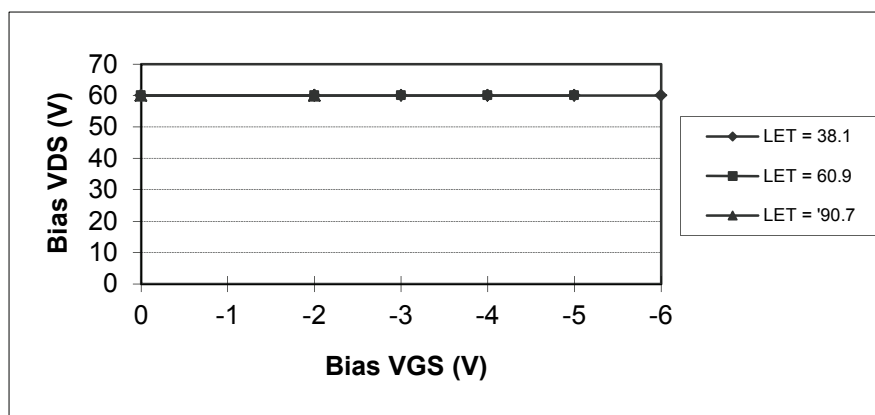
Symbol	Parameter	Up to 300 kRads (Si) <sup>1</sup>		Units	Test Conditions
		Min.	Max.		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	nA	V <sub>GS</sub> = 10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	nA	V <sub>GS</sub> = -10V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	1.0	μA	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source <sup>④</sup> On-State Resistance (TO-39)	—	0.65	Ω	V <sub>GS</sub> = 4.5V, I <sub>D2</sub> = 0.56A
R <sub>DS(on)</sub>	Static Drain-to-Source <sup>④</sup> On-State Resistance (LCC-6)	—	0.75	Ω	V <sub>GS</sub> = 4.5V, I <sub>D2</sub> = 0.56A
V <sub>SD</sub>	Diode Forward Voltage	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 0.89A

1. Part numbers IRHLUC770Z4 and IRHLUC730Z4

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

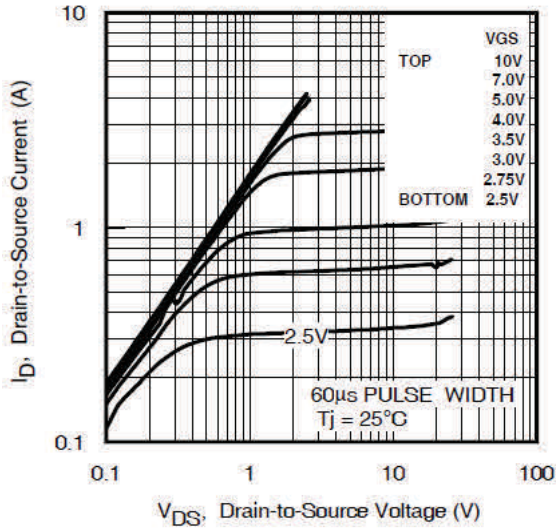
**Table 2. Typical Single Event Effect Safe Operating Area (Each N-Ch Die)**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)					
			@ VGS = 0V	@ VGS = -2V	@ VGS = -3V	@ VGS = -4V	@ VGS = -5V	@ VGS = -6V
38.1	358	43.9	60	60	60	60	60	60
60.9	659	54	60	60	60	60	60	—
90.7	1375	75.4	60	60	—	—	—	—

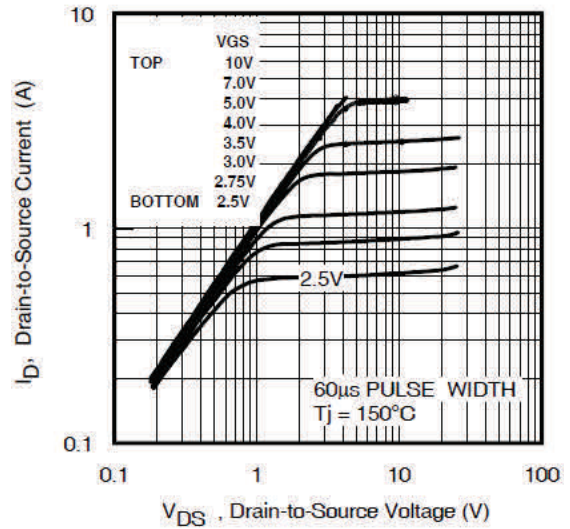


**Fig a.** Typical Single Event Effect, Safe Operating Area

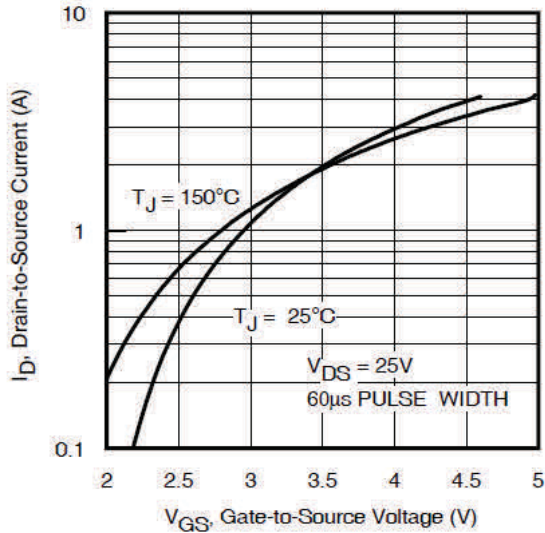
For Footnotes, refer to the page 2.



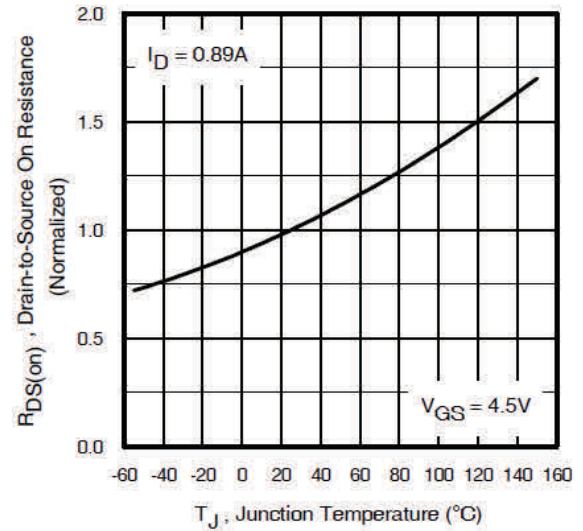
**Fig 1.** Typical Output Characteristics



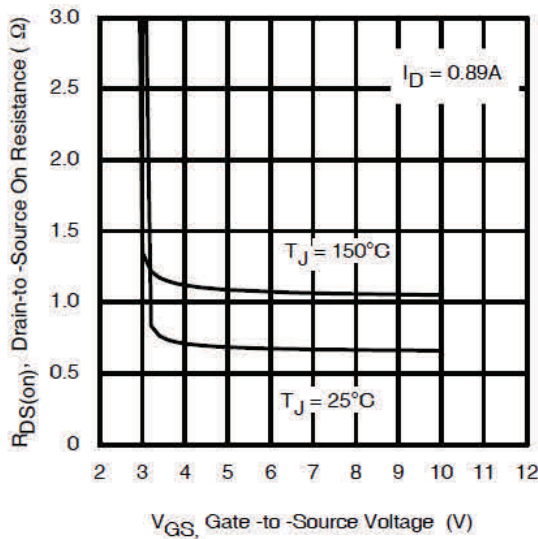
**Fig 2.** Typical Output Characteristics



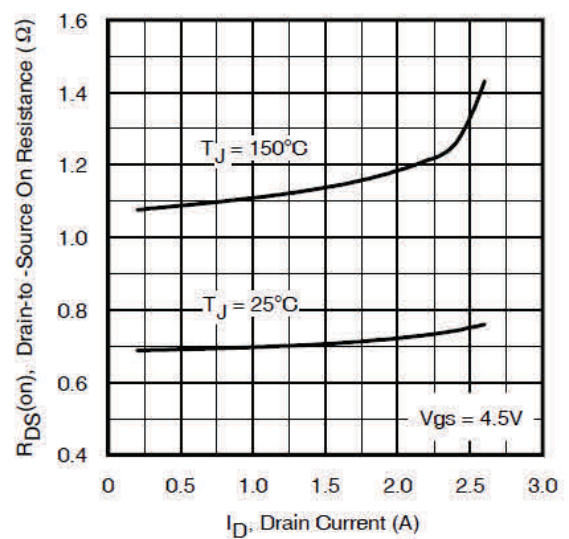
**Fig 3.** Typical Transfer Characteristics



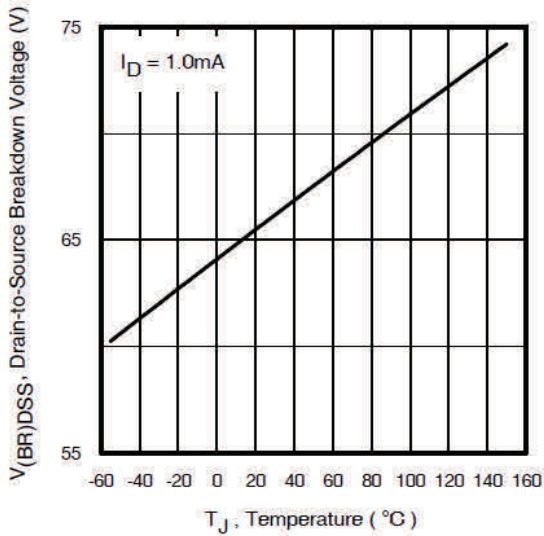
**Fig 4.** Normalized On-Resistance Vs. Temperature



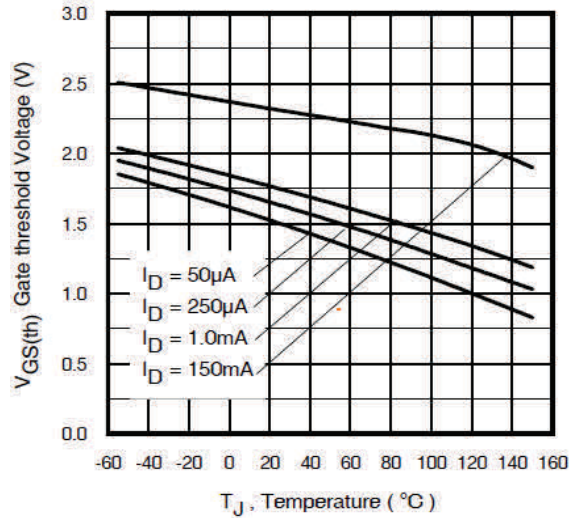
**Fig 5.** Typical On-Resistance Vs Gate Voltage



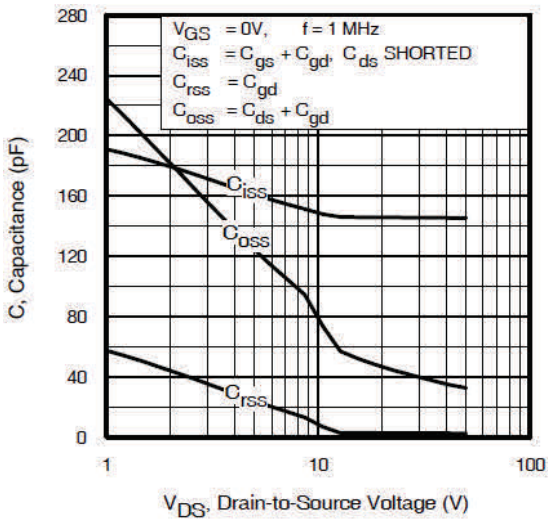
**Fig 6.** Typical On-Resistance Vs Drain Current



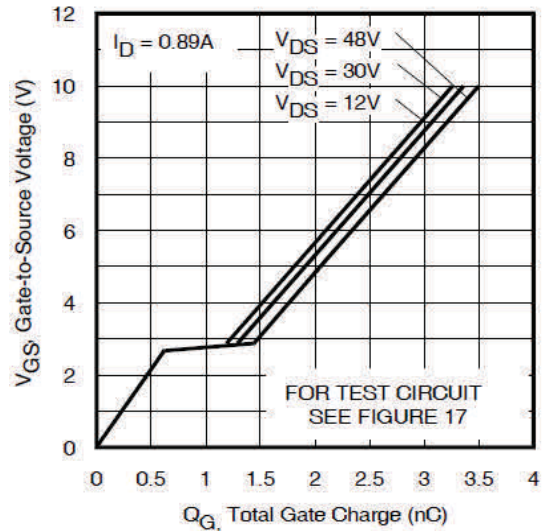
**Fig 7.** Typical Drain-to-Source Breakdown Voltage Vs Temperature



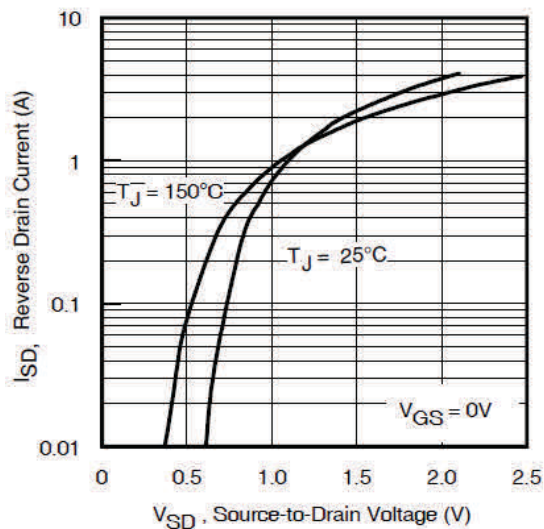
**Fig 8.** Typical Threshold Voltage Vs Temperature



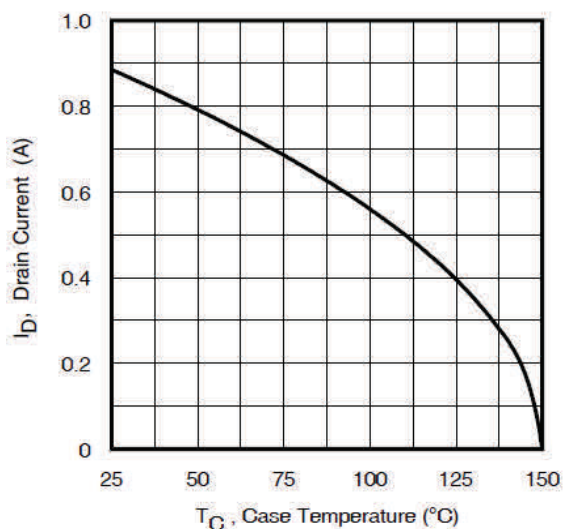
**Fig 9.** Typical Capacitance Vs. Drain-to-Source Voltage



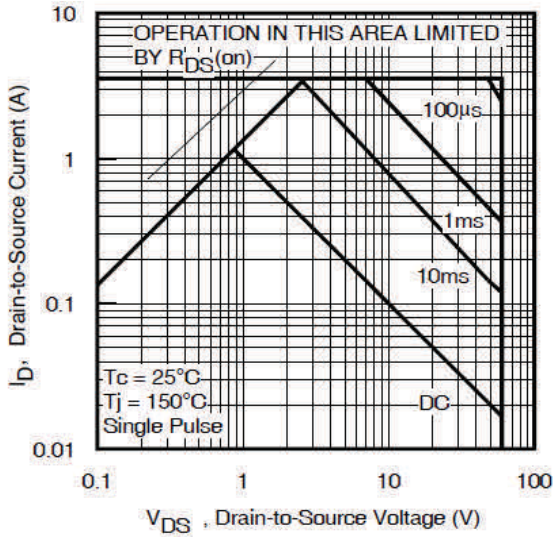
**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage



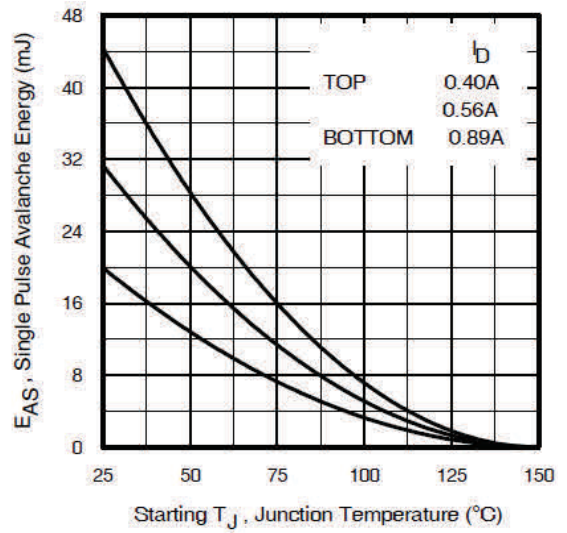
**Fig 11.** Typical Source-Drain Diode Forward Voltage



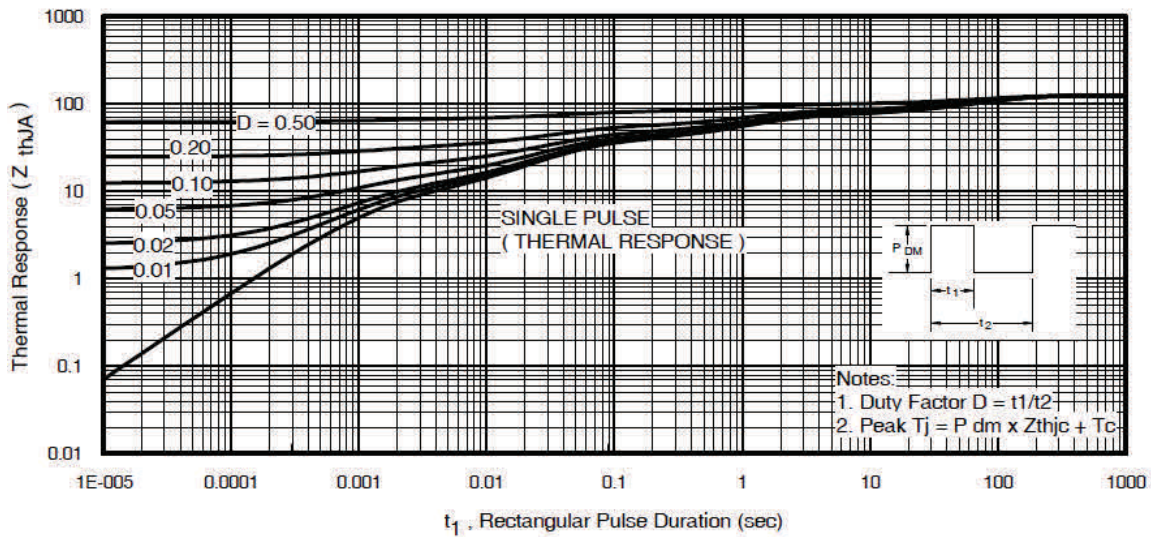
**Fig 12.** Maximum Drain Current Vs. Case Temperature



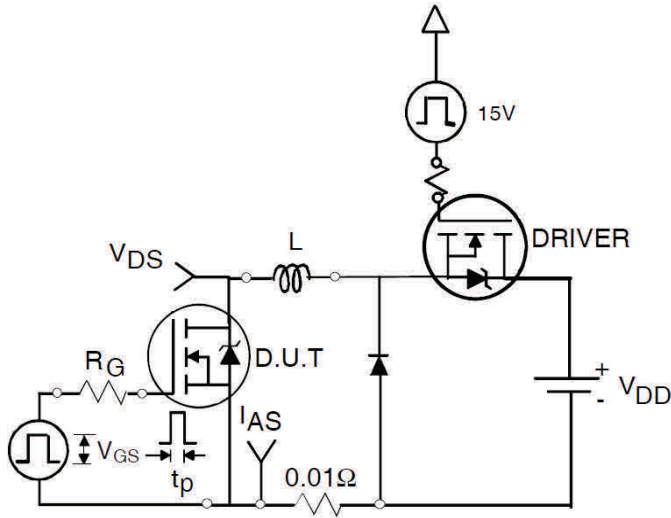
**Fig 13.** Maximum Safe Operating Area



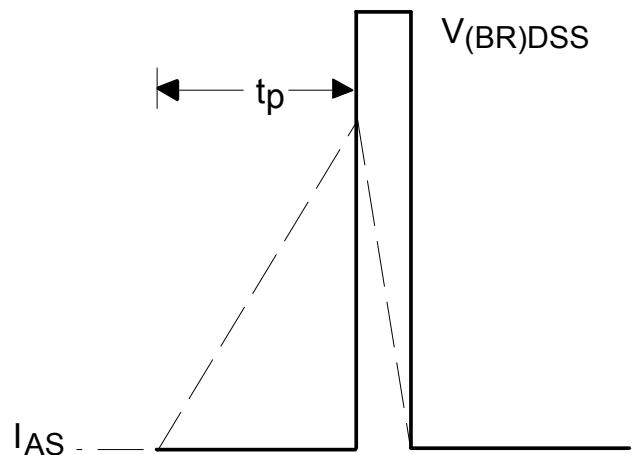
**Fig 14.** Maximum Avalanche Energy Vs. Drain Current



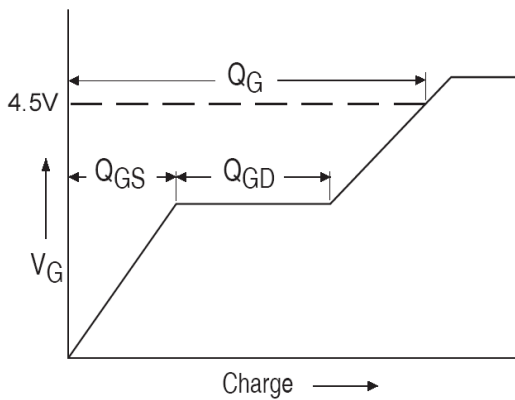
**Fig 15.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



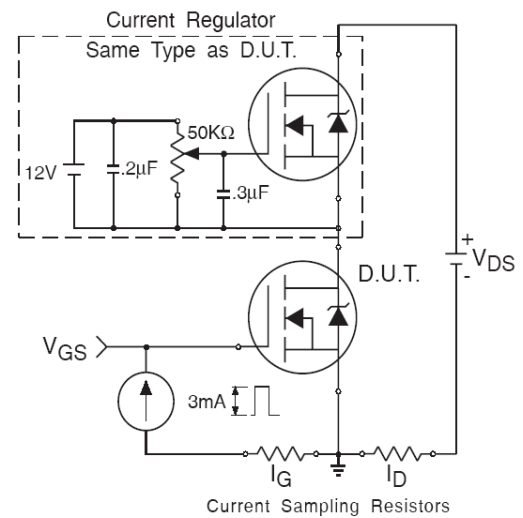
**Fig 16a.** Unclamped Inductive Test Circuit



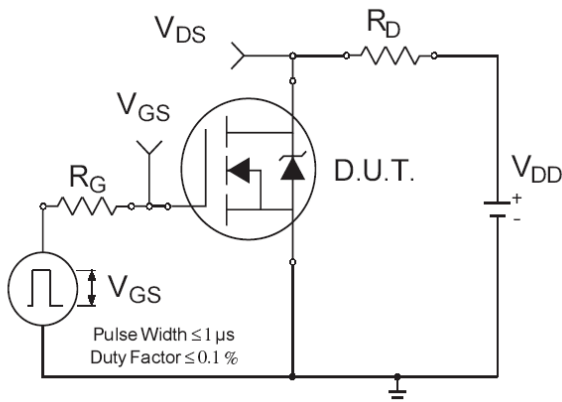
**Fig 16b.** Unclamped Inductive Waveforms



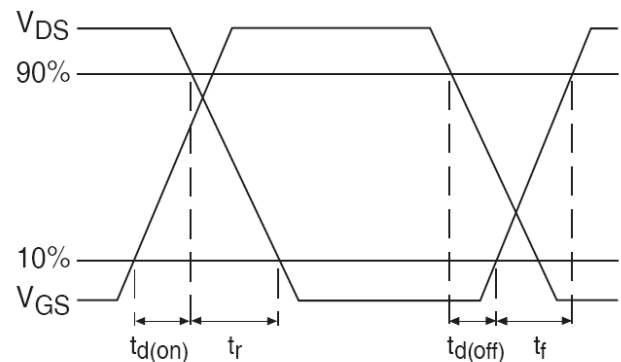
**Fig 17a.** Gate Charge Waveform



**Fig 17b.** Gate Charge Test Circuit

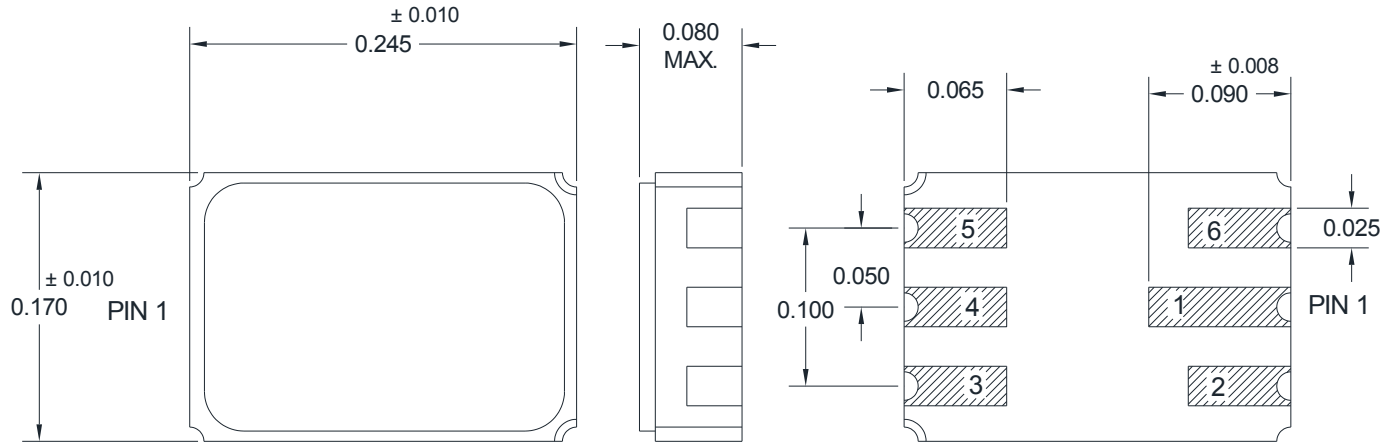


**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms

**Case Outline and Dimensions - LCC-6**



DIE 1 & 2 (N Ch)

	PIN #
DRAIN	- 1 & 4
GATE	- 2 & 5
SOURCE	- 6 & 3

**NOTES:**

1. OUTLINE CONFORMS TO MIL-PRF-19500/255L
2. ALL DIMENSIONS ARE SHOWN IN INCHES.



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