

## Normally – OFF Silicon Carbide Junction Transistor

$V_{DS}$	=	600 V
$R_{DS(ON)}$	=	425 mΩ
$I_D (T_c = 25^\circ C)$	=	10 A
$h_{FE} (T_c = 25^\circ C)$	=	110

### Features

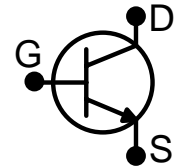
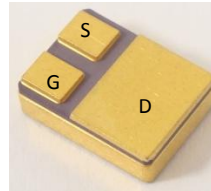
- 225°C maximum operating temperature
- Electrically Isolated Base Plate
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of  $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

### Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 μs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

### Package

- RoHS Compliant



SMD0.5 / TO – 276 (Hermetic Package)

### Applications

- Down Hole Oil Drilling
- Geothermal Instrumentation
- Solenoid Actuators
- General Purpose High-Temperature Switching
- Amplifiers
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)

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### Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	$V_{DS}$	$V_{GS} = 0 V$	600	V	
Continuous Drain Current	$I_D$	$T_J = 225^\circ C, T_C = 25^\circ C$	10	A	
Continuous Gate Current	$I_G$		0.5	A	
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 225^\circ C, I_G = 0.5 A,$ Clamped Inductive Load	$I_{D,max} = 10$ @ $V_{DS} \leq V_{DSmax}$	A	
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 225^\circ C, I_G = 0.5 A, V_{DS} = 400 V,$ Non Repetitive	>20	μs	
Reverse Gate – Source Voltage	$V_{SG}$		30	V	
Reverse Drain – Source Voltage	$V_{SD}$		25	V	
Power Dissipation	$P_{tot}$	$T_C = 25^\circ C, t_p > 100 ms$	125	W	
Storage Temperature	$T_{stg}$		-55 to 225	°C	

**Section II: Static Electrical Characteristics**

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
<b>A: On State</b>							
Drain – Source On Resistance	$R_{DS(on)}$	$I_D = 4\text{ A}, T_J = 25\text{ °C}$		425		mΩ	Fig. 5
		$I_D = 4\text{ A}, T_J = 175\text{ °C}$		800			
		$I_D = 4\text{ A}, T_J = 220\text{ °C}$		1180			
Gate – Source Saturation Voltage	$V_{GS,sat}$	$I_D = 5\text{ A}, I_D/I_G = 40, T_J = 25\text{ °C}$		3.45		V	Fig. 7
		$I_D = 5\text{ A}, I_D/I_G = 30, T_J = 175\text{ °C}$		3.22			
DC Current Gain	$h_{FE}$	$V_{DS} = 5\text{ V}, I_D = 5\text{ A}, T_J = 25\text{ °C}$	90	110		–	Fig. 5
		$V_{DS} = 5\text{ V}, I_D = 5\text{ A}, T_J = 220\text{ °C}$	60	80			
<b>B: Off State</b>							
Drain Leakage Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 25\text{ °C}$		0.1		μA	Fig. 8
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ °C}$		1			
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 220\text{ °C}$		10			
Gate Leakage Current	$I_{SG}$	$V_{SG} = 20\text{ V}, T_J = 25\text{ °C}$		20		nA	
<b>C: Thermal</b>							
Thermal resistance, junction - case	$R_{th(jc)}$			1.6		°C/W	

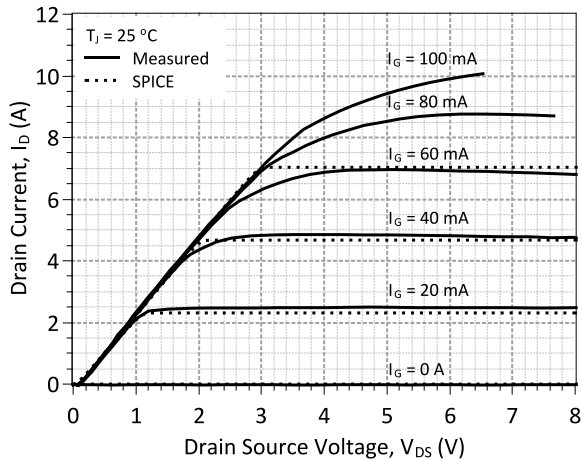
**Section III: Dynamic Electrical Characteristics**

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
<b>A: Capacitance and Gate Charge</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_D = 600\text{ V}, f = 1\text{ MHz}$		310		pF	Fig. 9
Reverse Transfer/Output Capacitance	$C_{rss}/C_{oss}$	$V_{DS} = 600\text{ V}, f = 1\text{ MHz}$		17		pF	Fig. 9
Output Capacitance Stored Energy	$E_{OSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, f = 1\text{ MHz}$		2.8		μJ	Fig. 10
Effective Output Capacitance, time related	$C_{oss,tr}$	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0...400\text{ V}$		27		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	$V_{GS} = 0\text{ V}, V_{DS} = 0...400\text{ V}$		21		pF	
Gate-Source Charge	$Q_{GS}$	$V_{GS} = -5...3\text{ V}$		3		nC	
Gate-Drain Charge	$Q_{GD}$	$V_{GS} = 0\text{ V}, V_{DS} = 0...400\text{ V}$		11		nC	
Gate Charge - Total	$Q_G$	$Q_{GS} + Q_{GD}$		14		nC	
<b>B: Switching<sup>1</sup></b>							
Internal Gate Resistance – zero bias	$R_{G(INT-ZERO)}$	$f = 1\text{ MHz}, V_{AC} = 50\text{ mV}, V_{DS} = 0\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ °C}$		14.5		Ω	
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	$V_{GS} > 2.5\text{ V}, V_{DS} = 0\text{ V}, T_J = 175\text{ °C}$		0.37		Ω	
Turn On Delay Time	$t_{d(on)}$	$T_J = 175\text{ °C}, V_{DS} = 400\text{ V}, I_D = 4\text{ A}, \text{Resistive Load}$		5		ns	
Fall Time, $V_{DS}$	$t_f$	Refer to Section V for additional driving information.		46		ns	Fig. 11
Turn Off Delay Time	$t_{d(off)}$			75		ns	
Rise Time, $V_{DS}$	$t_r$	$T_J = 225\text{ °C}, V_{DS} = 400\text{ V}, I_D = 4\text{ A}, \text{Resistive Load}$		19		ns	Fig. 12
Turn On Delay Time	$t_{d(on)}$			10		ns	
Fall Time, $V_{DS}$	$t_f$	$T_J = 225\text{ °C}, V_{DS} = 400\text{ V}, I_D = 4\text{ A}, \text{Resistive Load}$		46		ns	Fig. 11
Turn Off Delay Time	$t_{d(off)}$			115		ns	
Rise Time, $V_{DS}$	$t_r$	$T_J = 175\text{ °C}, V_{DS} = 400\text{ V}, I_D = 4\text{ A}, \text{Inductive Load}$		18		ns	Fig. 12
Turn-On Energy Per Pulse	$E_{on}$			24		μJ	Fig. 11
Turn-Off Energy Per Pulse	$E_{off}$	Refer to Section V.		8		μJ	Fig. 12,
Total Switching Energy	$E_{tot}$			32		μJ	
Turn-On Energy Per Pulse	$E_{on}$	$T_J = 225\text{ °C}, V_{DS} = 400\text{ V}, I_D = 4\text{ A}, \text{Inductive Load}$		31		μJ	Fig. 11
Turn-Off Energy Per Pulse	$E_{off}$			9		μJ	Fig. 12
Total Switching Energy	$E_{tot}$			40		μJ	

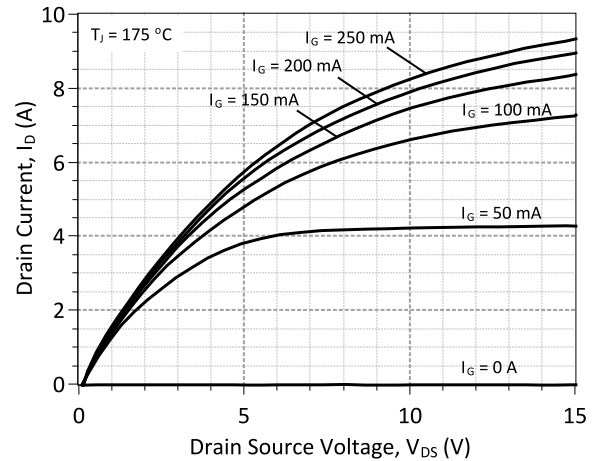
<sup>1</sup> – All times are relative to the Drain-Source Voltage  $V_{DS}$

**Section IV: Figures**

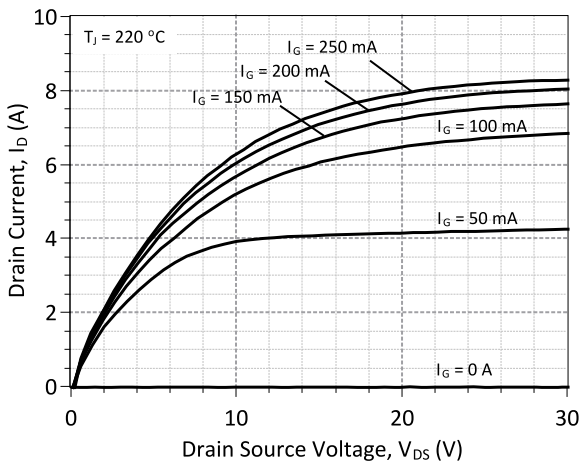
**A: Static Characteristic**



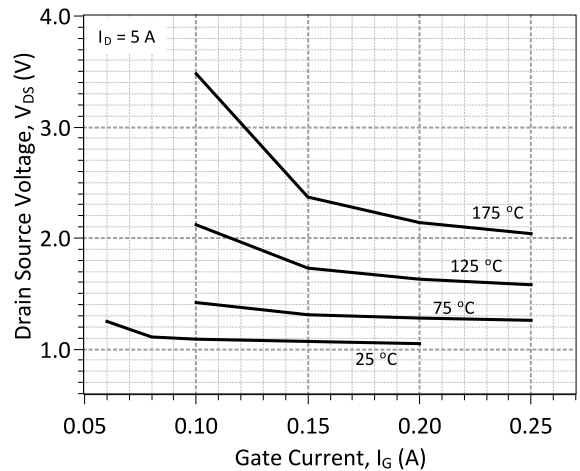
**Figure 1: Typical Output Characteristics at 25 °C**



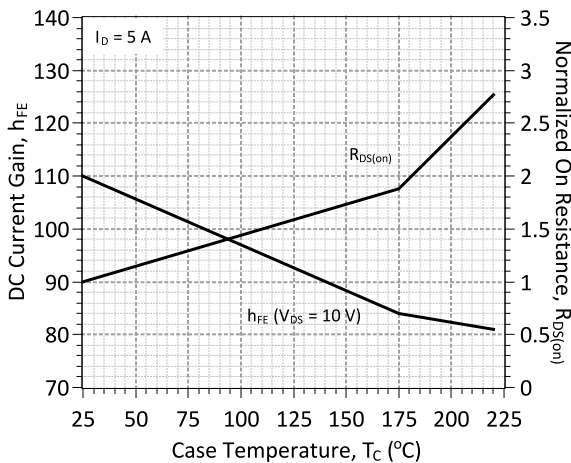
**Figure 2: Typical Output Characteristics at 175 °C**



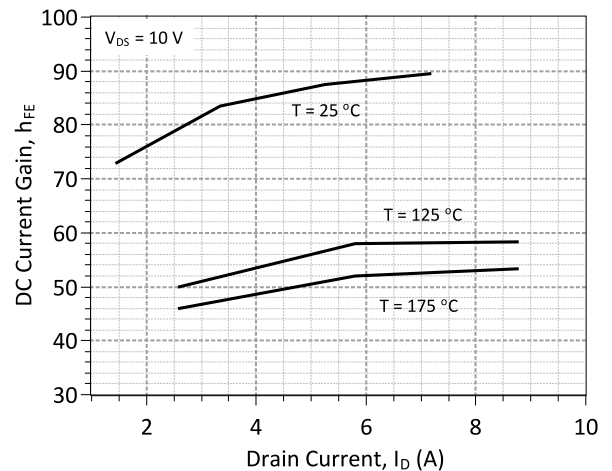
**Figure 3: Typical Output Characteristics at 220 °C**



**Figure 4: Drain-Source Voltage vs. Gate Current**



**Figure 5: DC Current Gain and Normalized On-Resistance vs. Temperature**



**Figure 6: DC Current Gain vs. Drain Current**

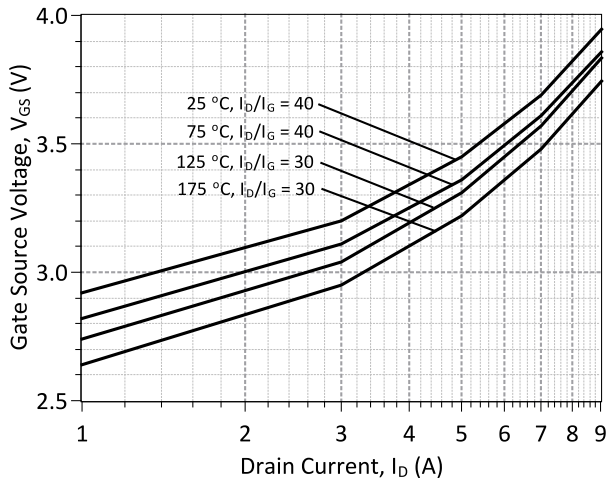


Figure 7: Typical Gate – Source Saturation Voltage

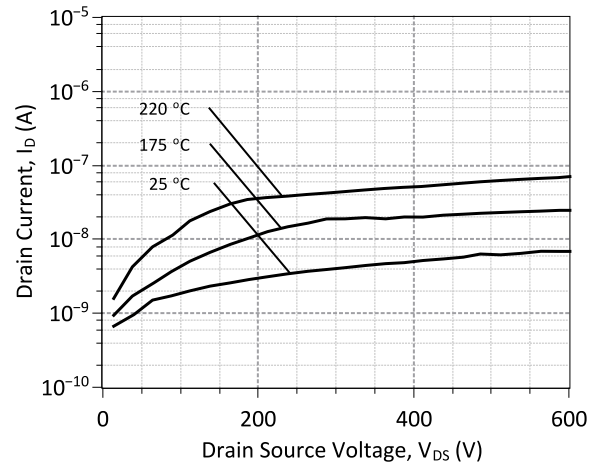


Figure 8: Typical Blocking Characteristics

**B: Dynamic Characteristic Figures**

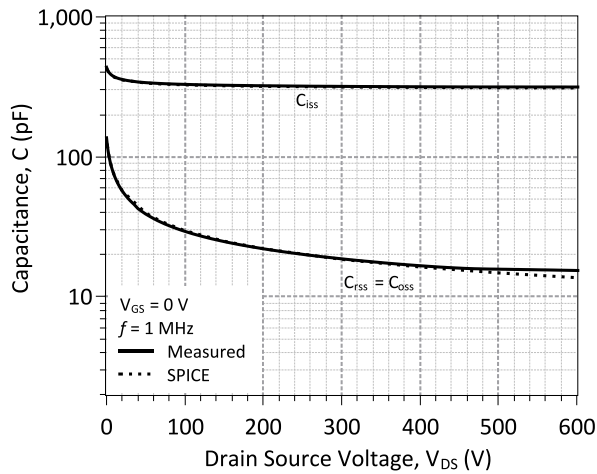


Figure 9: Input, Output, and Reverse Transfer Capacitance

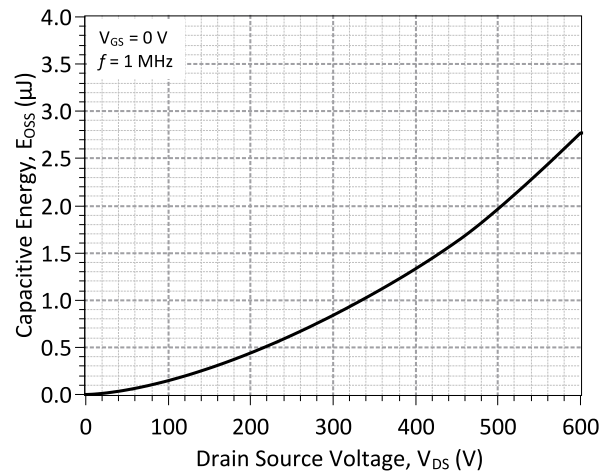


Figure 10: Output Capacitance Stored Energy

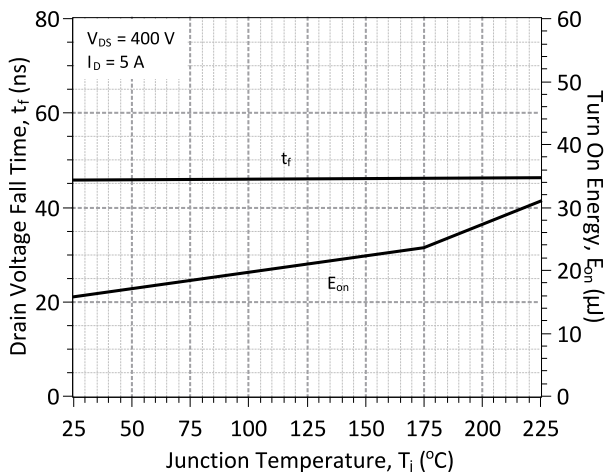


Figure 11: Typical Switching Times and Turn On Energy Losses vs. Temperature

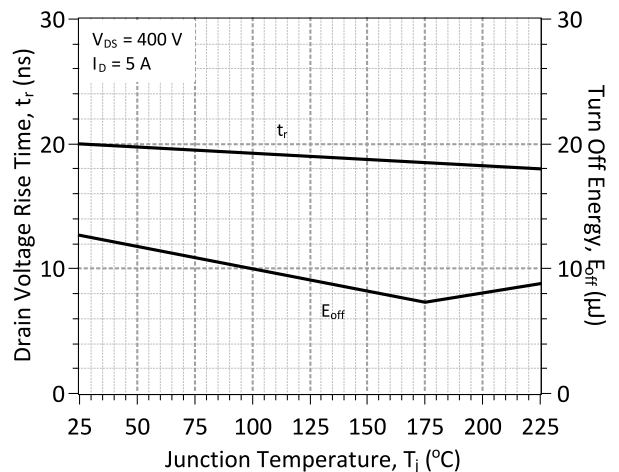
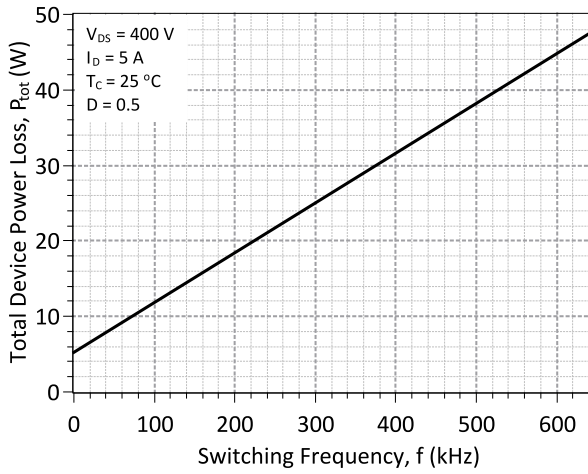
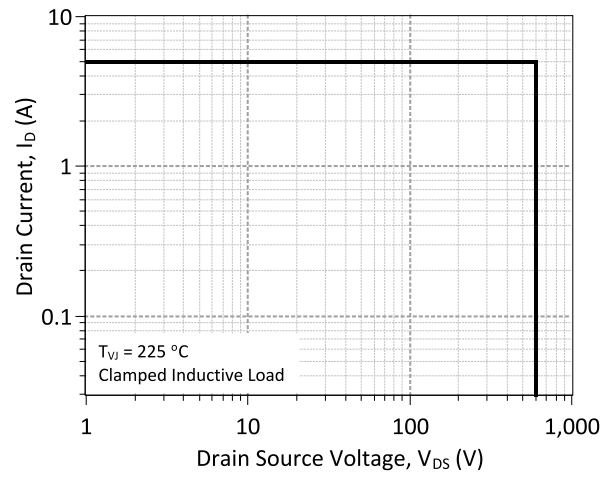


Figure 12: Typical Switching Times and Turn Off Energy Losses vs. Temperature



**Figure 13: Typical Hard Switched Device Power Loss vs. Switching Frequency<sup>2</sup>**



**Figure 14: Turn-Off Safe Operating Area**

## Section V: Driving the 2N7636-GA

The 2N7636-GA is a current controlled SiC transistor which requires a positive gate current for turn-on and to remain in on-state. It may be driven by different drive topologies depending on the intended application.

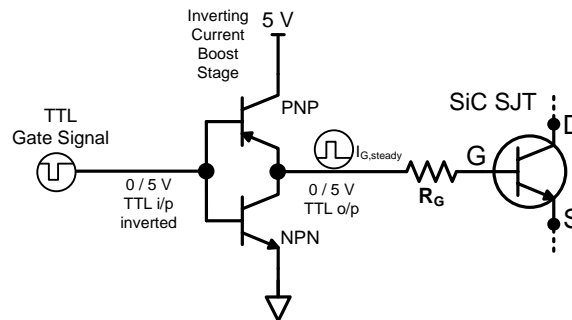
**Table 1: Estimated Power Consumption and switching frequencies for various Gate Drive topologies.**

Drive Topology	Gate Drive Power Consumption	Switching Frequency
Simple TTL	High	Low
Constant Current	Medium	Medium
High Speed – Boost Capacitor	Medium	High
High Speed – Boost Inductor	Low	High
Proportional	Lowest	Medium
Pulsed Power	Medium	N/A

### A: Simple TTL Drive

The 2N7636-GA may be driven by 5 V TTL logic by using a simple current amplification stage. The current amplifier output current must meet or exceed the steady state gate current,  $I_{G,steady}$ , required to operate the 2N7636-GA. An external gate resistor  $R_G$ , shown in the Figure 15 topology, sets  $I_{G,steady}$  to the required level which is dependent on the SJT drain current  $I_D$  and DC current gain  $h_{FE}$ .  $R_G$  may be calculated from the equation below. The value of  $V_{EC,sat}$  can be taken from the PNP datasheet, a partial list of high-temperature PNP and NPN transistors options is given below. High-temperature MOSFETs may also be used in the topology.

$$R_{G,max} = \frac{(5.0\text{ V} - V_{EC,sat}(PNP) - V_{GS,sat}(SJT)) * h_{FE}(T, I_D)}{I_D * 1.5}$$



**Figure 15: Simple TTL Gate Drive Topology**

**Table 2: Partial List of High-Temperature BJTs for TTL Gate Driving**

BJT Part Number	Type	$T_{j,max}$ (°C)
PHPT60603PY	PNP	175
PHPT60603NY	NPN	175
2N2222	NPN	200
2N6730	PNP	200
2N2905	PNP	200
2N5883	PNP	200
2N5885	NPN	200

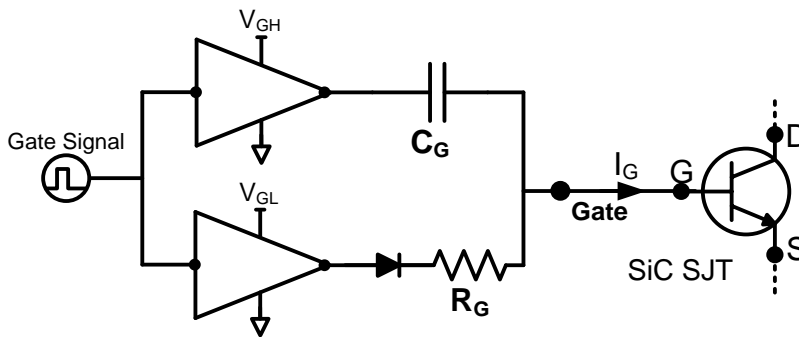
**B: High Speed Driving**

For ultra high speed 2N7636-GA switching ( $t_r, t_f < 20$  ns) while maintaining low gate drive losses the supplied gate current should include a positive current peak during turn-on, a negative voltage peak during turn-off, and continuous gate current  $I_G$  to remain on.

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge for turn-on,  $Q_G$ , is supplied by a burst of high gate current until the gate-source capacitance,  $C_{GS}$ , and gate-drain capacitance,  $C_{GD}$ , are fully charged. Ideally, the burst should terminate when the drain voltage has fallen to its on-state value in order to avoid unnecessary drive losses. A negative voltage peak is recommended for the turn-off transition in order to ensure that the gate current is not being supplied under high  $dV/dt$  due to the Miller effect. While satisfactory turn off can be achieved with  $V_{GS} = 0$  V, a negative  $V_{GS}$  value may be used in order to speed up the turn-off transition.

**B:1: High Speed, Low Loss Drive with Boost Capacitor**

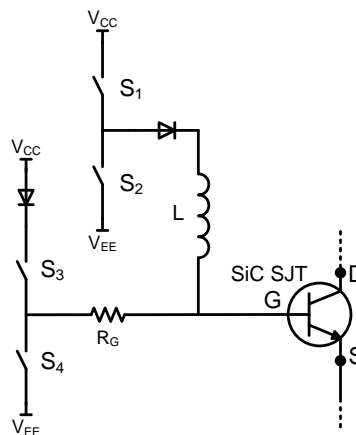
The 2N7636-GA may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide current peaks at turn-on and turn-off for fast switching and a continuous gate current while in on-state. As shown in Figure 16, in this topology two gate driver ICs are utilized. An external gate resistor  $R_G$  is driven by a low voltage driver to supply the continuous gate current throughout on-state, and a gate capacitor  $C_G$  is driven at a higher voltage level to supply a high current peak at turn-on and turn-off. A 3 kV isolated evaluation gate drive board (GA03IDDJT30-FR4) from GeneSiC Semiconductor utilizing this topology is commercially available for high and low-side driving, its datasheet provides additional details about this drive topology.



**Figure 16: High Speed, Low Loss Drive with Boost Capacitor Topology**

**B:2: High Speed, Low Loss Drive with Boost Inductor**

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the 2N7636-GA at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses  $I_{G,on}$  and  $I_{G,off}$ . During operation, inductor  $L$  is charged to a specified  $I_{G,on}$  current value then made to discharge  $I_L$  into the SJT gate pin using logic control of  $S_1, S_2, S_3$ , and  $S_4$ , as shown in Figure 17. After turn on, while the device remains on the necessary steady state gate current  $I_{G,steady}$  is supplied from source  $V_{CC}$  through  $R_G$ . Please refer to the article "A current-source concept for fast and efficient driving of silicon carbide transistors" by Dr. Jacek Rąbkowski for additional information on this driving topology.<sup>3</sup>



**Figure 17: High Speed, Low-Loss Driver with Boost Inductor Topology**

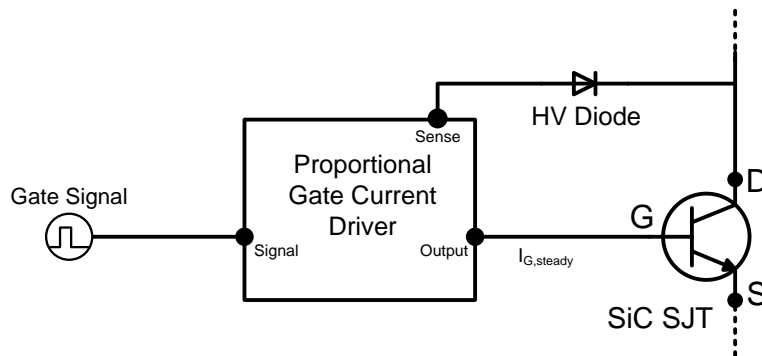
<sup>3</sup> – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/ae-2013-0026, June 2013

**C: Proportional Gate Current Driving**

A proportional gate drive topology may be beneficial for applications in which the 2N7636-GA will operate over a wide range of drain current conditions to lower the gate drive power consumption. A proportional gate driver relies on instantaneous drain current  $I_D$  feedback to vary the steady state gate current  $I_{G,steady}$  supplied to the 2N7636-GA.

**C:1: Voltage Controlled Proportional Driver**

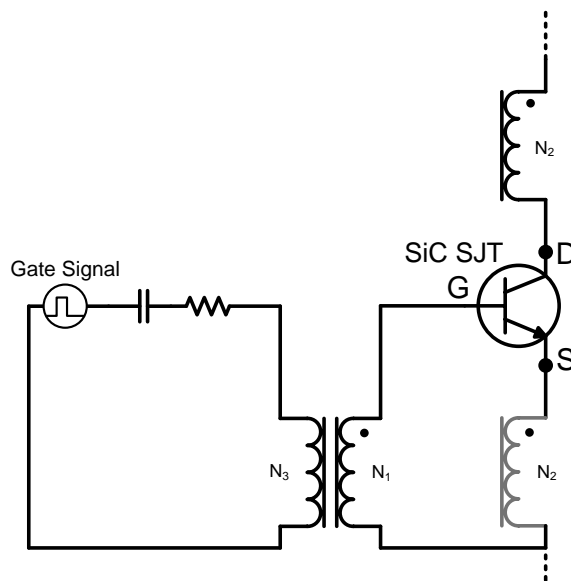
A voltage controlled proportional driver relies on a gate drive integrated circuit to detect the 2N7636-GA drain-source voltage  $V_{DS}$  during on-state to sense  $I_D$ . The integrated circuit will then increase or decrease  $I_G$  in response to  $I_D$ . This allows  $I_G$  and gate drive power consumption to reduce while  $I_D$  is low or for  $I_G$  to increase when  $I_D$  increases. A high voltage diode connected between the drain and sense protects the integrated circuit from high-voltage when blocking. A simplified version of this topology is shown in Figure 18. Additional information will be available in the future at <http://www.genesicsemi.com/references/product-notes/>.



**Figure 18: Simplified Voltage Controlled Proportional Driver**

**C:2: Current Controlled Proportional Driver**

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback of the 2N7636-GA drain current during on-state to supply  $I_{G,steady}$  into the gate.  $I_{G,steady}$  will increase or decrease in response to  $I_D$  at a fixed forced current gain which is set by the turns ratio of the transformer,  $h_{force} = I_D / I_G = N_2 / N_1$ . 2N7636-GA is initially tuned-on using a gate current pulse supplied into an RC drive circuit to allow  $I_D$  current to begin flowing. This topology allows  $I_{G,steady}$  and the gate drive power consumption to reduce while  $I_D$  is relatively low or for  $I_{G,steady}$  to increase when  $I_D$  increases. A simplified version of this topology is shown in Figure 19. Additional information will be available in the future at <http://www.genesicsemi.com/references/product-notes/>.

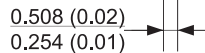
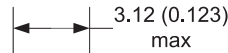
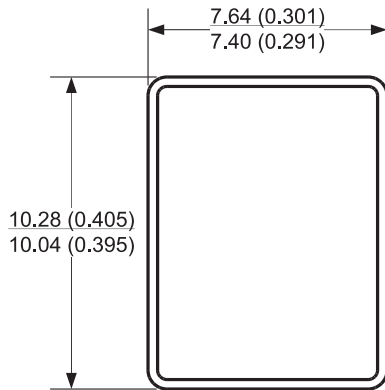


**Figure 19: Simplified Current Controlled Proportional Driver**

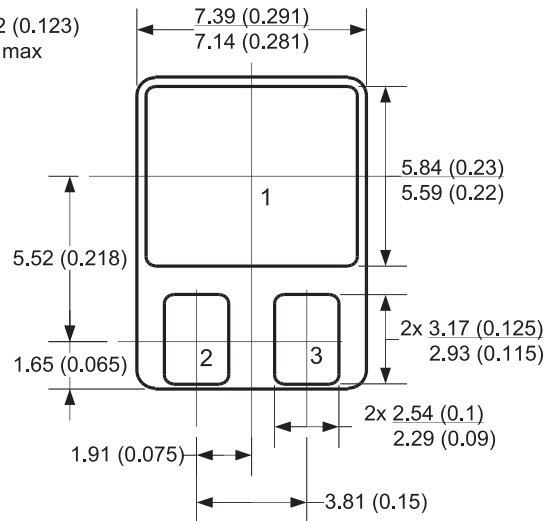


Section VI: Package Dimensions

SMD-0.5/TO-276



PACKAGE OUTLINE



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2014/12/12	6	Updated Electrical Characteristics	
2014/08/23	5	Updated Electrical Characteristics	
2014/03/20	4	Updated Gate Drive Section	
2014/02/11	3	Updated Electrical Characteristics	
2013/12/19	2	Updated Gate Drive Section	
2013/11/18	1	Updated Electrical Characteristics	
2012/08/24	0	Initial release	

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**Section VII: SPICE Model Parameters**

This is a secure document. Please copy this code from the SPICE model PDF file on our website ([http://www.genesicsemi.com/images/hit\\_sic/sjt/2N7636-GA\\_SPICE.pdf](http://www.genesicsemi.com/images/hit_sic/sjt/2N7636-GA_SPICE.pdf)) into LTSPICE (version 4) software for simulation of the 2N7636-GA.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   1.2           $
*      $Date:      23-JUN-2014   $
*
*      GeneSiC Semiconductor Inc.
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*      Dulles, VA 20166
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*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model 2N7636 NPN
+ IS      1.22E-47
+ ISE     3.908E-27
+ EG      3.23
+ BF      121
+ BR      0.55
+ IKF     999
+ NF      1
+ NE      2.022
+ RB      10.0
+ RE      0.231
+ RC      0.16
+ CJC     1.37E-10
+ VJC     3.150960833
+ MJC     0.43821105
+ CJE     2.97E-10
+ VJE     2.901930244
+ MJE     0.475141754
+ XTI     3
+ XTB     -0.45
+ TRC1    1.50E-02
+ VCEO    600
+ ICRATING 10
+ MFG     GeneSiC_Semiconductor
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* End of 2N7636-GA SPICE Model
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