2N964 (GERMANIUM)

For Specifications, See 2N960 Data.

2N964A (GERMANIUM)

PNP germanium epitaxial mesa transistor for high-speed switching applications.

CASE 22
(TO-18)
Collector Connected to Case

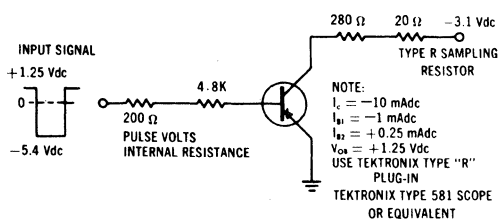
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	7.0	Vdc
Collector-Base Voltage	V_{CB}	15	Vdc
Emitter-Base Voltage	V_{EB}	2.5	Vdc
Collector Current	I_C	100	mAdc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	150 2.0	mW $mW/^oC$
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	300 4.0	mW $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +100	^oC

THERMAL CHARACTERISTICS

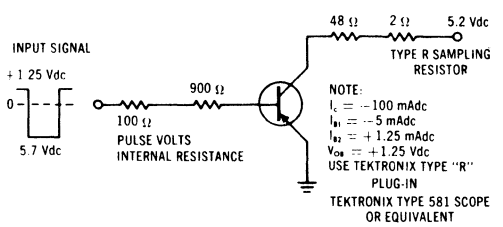
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.25	$^oC/mW$
Thermal Resistance, Case to Ambient	θ_{CA}	0.5	$^oC/mW$

FIGURE 1



10-mA (I_C) SWITCHING TIME TEST CIRCUIT

FIGURE 2



100-mA (I_C) SWITCHING TIME TEST CIRCUIT

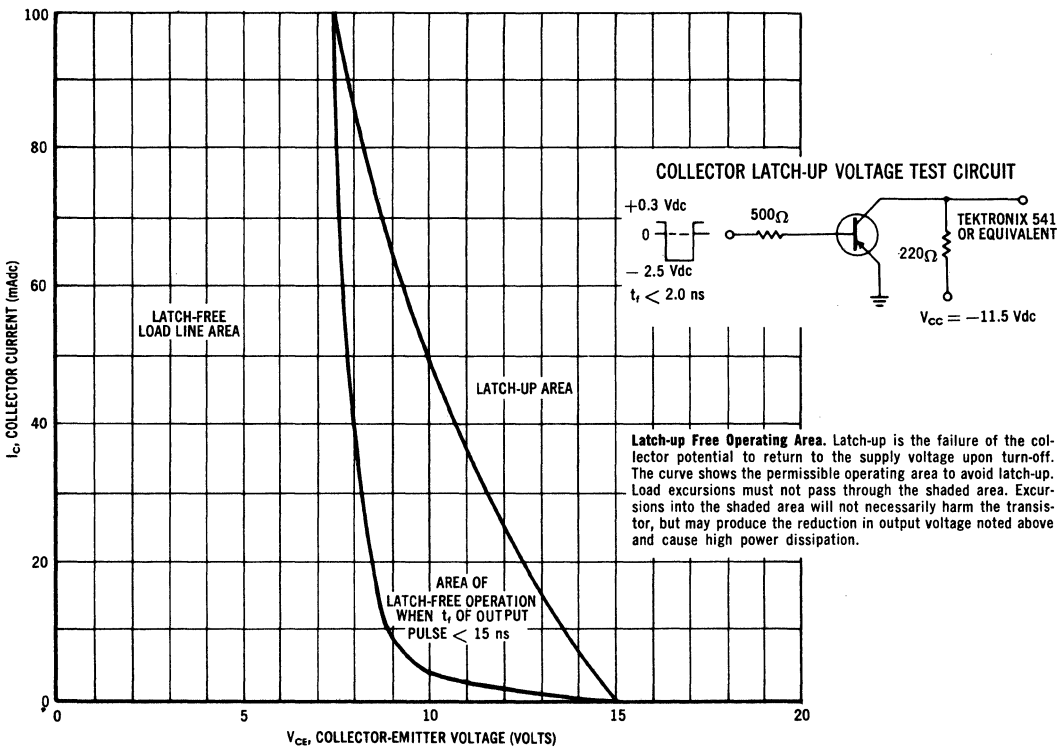
2N964A (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)		BV_{CEO}	7.0	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	15	25	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	2.5	-	-	Vdc
Collector Latch-up Voltage	3	LV_{CEX}	11.5	-	-	Vdc
Collector-Emitter Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)		I_{CES}	-	-	100	μAdc
Collector Cutoff Current (V_{CB} = 6 Vdc, I_E = 0)		I_{CBO}	-	0.4	3.0	μAdc
Base Leakage Current (V_{CE} = 6 Vdc, $V_{BE(off)}$ = 0.5 Vdc)	4	I_{BL}	-	-	4.0	μAdc
(V_{CE} = 6 Vdc, $V_{BE(off)}$ = 0.5 Vdc, T_J = 85°C)			-	50	140	
ON CHARACTERISTICS						
DC Current Gain	8	h_{FE}				
(I_C = 10 mAdc, V_{CE} = 0.3 Vdc)			40	80	-	
(I_C = 10 mAdc, V_{CE} = 0.3 Vdc, T_J = -55°C)			20	45	-	
(I_C = 50 mAdc, V_{CE} = 1 Vdc)			48	105	-	
(I_C = 100 mAdc, V_{CE} = 1 Vdc)			40	95	-	
(I_C = 100 mAdc, V_{CE} = 1 Vdc, T_J = 85°C)			35	85	-	
Collector Saturation Voltage	5	$V_{CE(sat)}$				Vdc
(I_C = 10 mAdc, I_B = 1 mAdc)			-	0.1	0.18	
(I_C = 50 mAdc, I_B = 5 mAdc)			-	0.16	0.28	
(I_C = 100 mAdc, I_B = 10 mAdc)			-	0.22	0.4	
Base-Emitter Saturation Voltage	6	$V_{BE(sat)}$				Vdc
(I_C = 10 mAdc, I_B = 1 mAdc)			0.3	0.38	0.44	
(I_C = 50 mAdc, I_B = 5 mAdc)			0.4	0.48	0.58	
(I_C = 100 mAdc, I_B = 10 mAdc)			0.4	0.6	0.72	
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_E = 20 mAdc, V_{CB} = 1 Vdc, f = 100 MHz)		f_T	300	460	-	MHz
High-Frequency Current Gain (I_C = 20 mAdc, V_{CE} = 1 Vdc, f = 100 MHz)		h_{fe}	3.0	4.6	-	-
Output Capacitance	11	C_{ob}				pF
(V_{CB} = 1 Vdc, I_E = 0, f = 1 MHz)			-	2.7	5.0	
(V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			-	2.2	4.0	
Input Capacitance (V_{BE} = 1 Vdc, I_C = 0, f = 100 kHz)	11	C_{ib}	-	2.0	3.5	pF
Delay Time Plus Rise Time		$t_d + t_r$				ns
(I_C = 10 mAdc)	1		-	35	50	
(I_C = 100 mAdc)	2		-	30	50	
Storage Time Plus Fall Time		$t_s + t_f$				ns
(I_C = 10 mAdc)	1		-	60	85	
(I_C = 100 mAdc)	2		-	50	85	
Active Region Time Constant (I_C = 10 mAdc)	9	τ_A	-	0.6	1.5	ns
Total Control Charge (I_C = 10 mAdc, I_B = 1 mAdc)	10	Q_T	-	50	75	pC

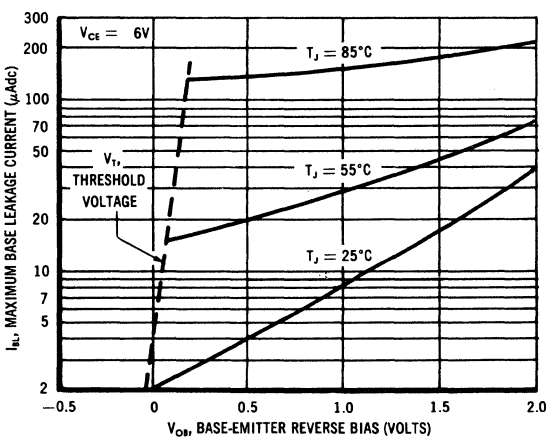
2N964A LIMIT CURVES

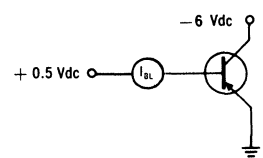
FIGURE 3—AREA OF PERMISSIBLE LOAD LOCI



Latch-up Free Operating Area. Latch-up is the failure of the collector potential to return to the supply voltage upon turn-off. The curve shows the permissible operating area to avoid latch-up. Load excursions must not pass through the shaded area. Excursions into the shaded area will not necessarily harm the transistor, but may produce the reduction in output voltage noted above and cause high power dissipation.

FIGURE 4—COMMON EMITTER DC LEAKAGE CHARACTERISTICS





BASE LEAKAGE CURRENT TEST CIRCUIT

Base Leakage Current. I_{BL} is defined as base leakage current with both junctions reverse biased. I_c is always less than I_{BL} for $V_{OB} > V_T$. (V_{OB} is off condition base bias, V_T is base voltage at threshold of conduction.)

NOTE: Limit Curves are based on periodic engineering evaluation. Production Tests are made at points indicated in the Electrical Characteristics Table.

2N964A LIMIT CURVES

FIGURE 5—COLLECTOR-EMITTER SATURATION VOLTAGE versus BASE CURRENT

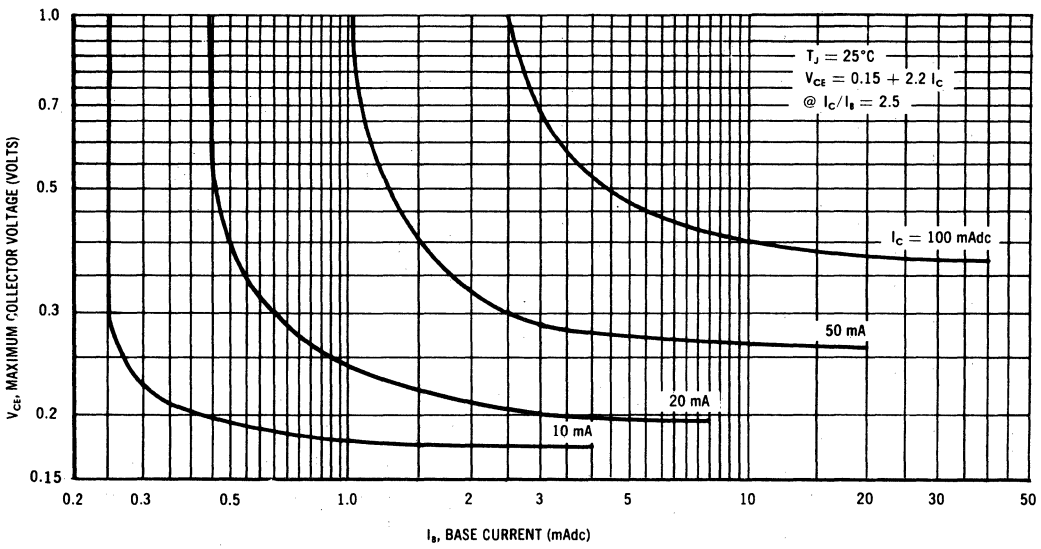


FIGURE 6—BASE-EMITTER VOLTAGE versus COLLECTOR CURRENT

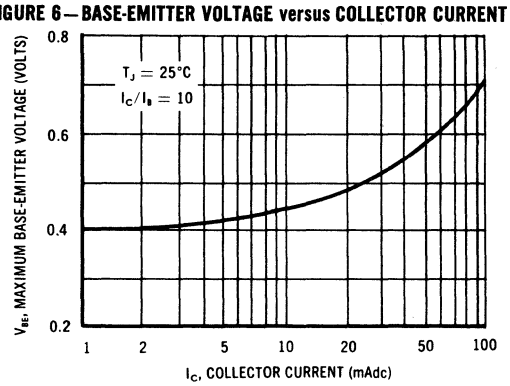


FIGURE 7—TEMPERATURE CO-EFFICIENTS

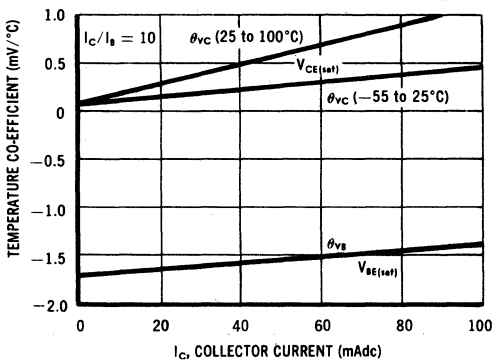


FIGURE 8—CURRENT GAIN CHARACTERISTICS

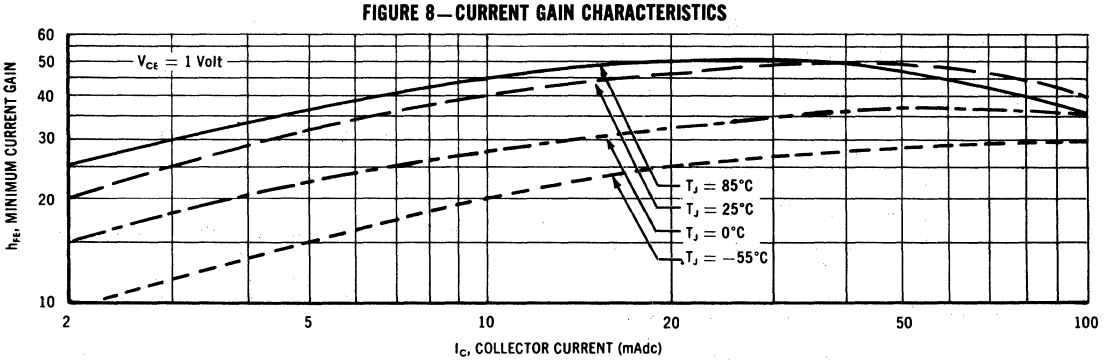


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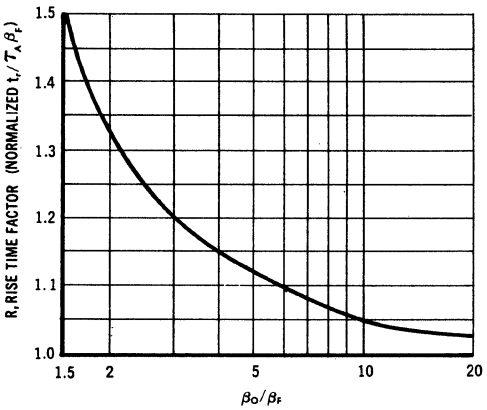
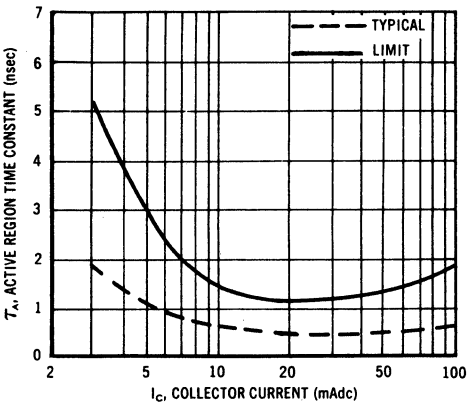
FIGURE 9—SWITCHING TIME CURVES FOR RESISTOR COUPLED CIRCUITS

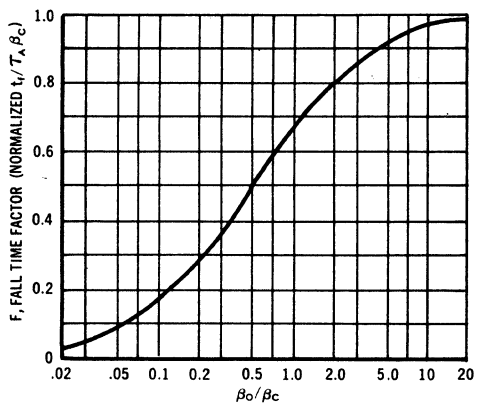
9a—RISE TIME FACTOR



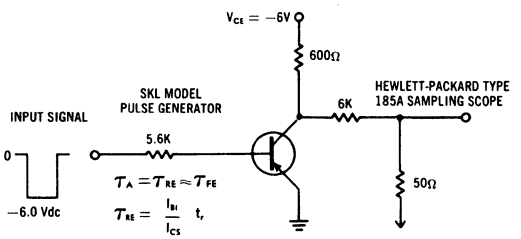
9b—ACTIVE REGION TIME CONSTANT



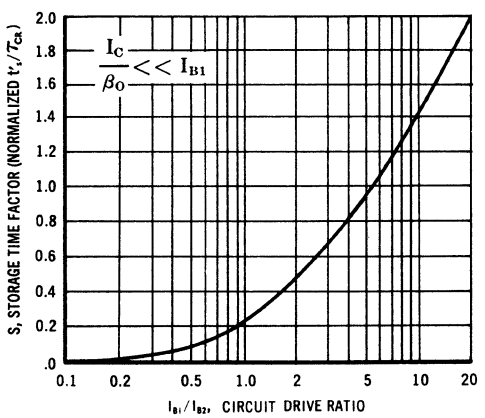
9c— FALL TIME FACTOR



ACTIVE REGION TIME CONSTANT TEST CIRCUIT



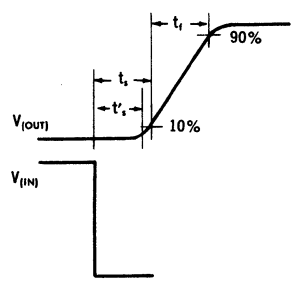
9d—STORAGE TIME



SWITCHING TIME EQUATIONS

RISE-TIME $= t_r = \tau_A\beta_F R$
FALL-TIME $= t_f = \tau_A\beta_C F$
STORAGE TIME $= t'_s = \tau_{CR} S$
t_r = 10 to 90% rise-time
t_f = 10 to 90% fall-time
$t_s = t'_s + \frac{1}{8} t_f$
τ_{CR} = the effective collector recovery time and is virtually uninfluenced by current levels. 20 ns typical and 60 ns maximum for this transistor.

τ_A = active region time constant
$\tau_A = \tau_{RE} \approx \tau_{FE}$ (Figure 9b)
$\beta_O = h_{FE}$ at edge of saturation ($\beta_O \approx h_{FE}$ on Figure 8)
$\beta_F = I_C$ in saturation/I_{B1} (base "on" current)
$\beta_C = I_C$ in saturation/I_{B2} (base "off" current)
R see Figure 9a
F see Figure 9c
S see Figure 9d



NOTE: Limit Curves are based on periodic engineering evaluation. Production Tests are made at points indicated in the Electrical Characteristics Table.

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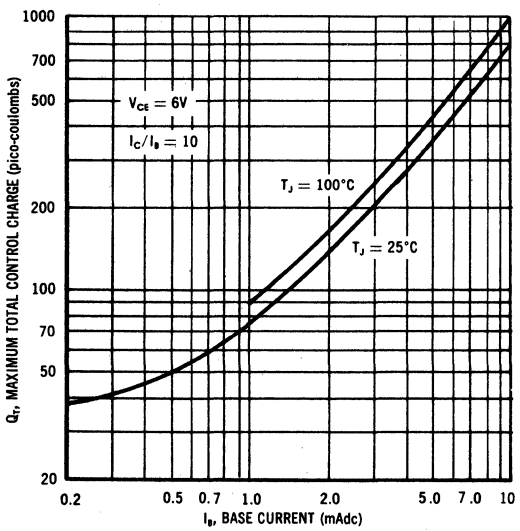
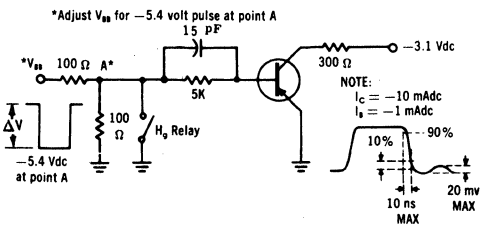
FIGURE 10—TOTAL CONTROL CHARGE



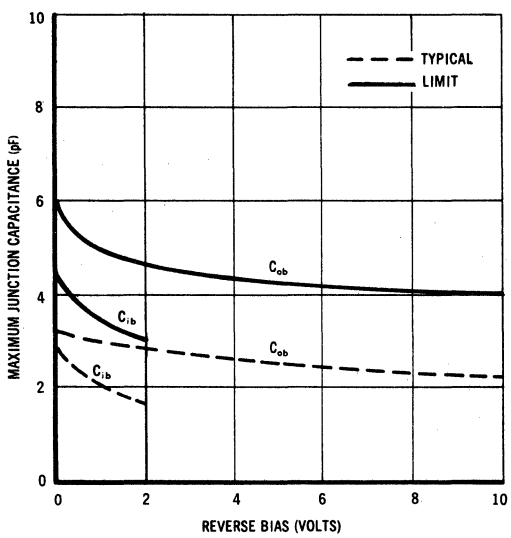
10a



10b

Total Control Charge. When a transistor is held in a conductive state by a current, I_{B1}, a charge Q_S is developed in the active region. A charge Q_T of opposite polarity, equal in magnitude, can be stored on an external capacitor C to neutralize the internal charge and considerably reduce the turn-off time of the transistor. Figure 10b shows the test circuit and turn-off waveform. Given Q_T from Figure 10a, the external C for worst case turn-off in any circuit is: $C = Q_T/\Delta V$, where ΔV is defined in Figure 10b.

FIGURE 11— JUNCTION CAPACITANCE VARIATIONS



NOTE: Limit Curves are based on periodic engineering evaluation. Production Tests are made at points indicated in the Electrical Characteristics Table.