RENESAS

SILICON POWER TRANSISTOR
2SA1741

PNP SILICON EPITAXIAL TRANSISTOR FOR HIGH-SPEED SWITCHING

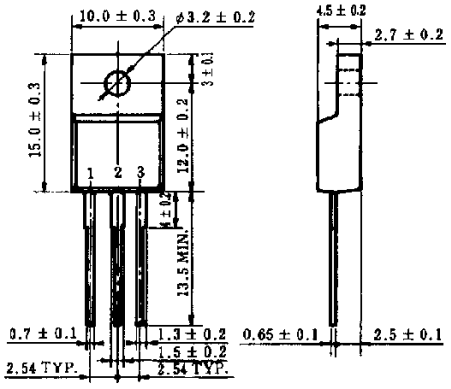
The 2SA1741 is a power transistor developed for high-speed switching and features a high h_{FE} at low $V_{CE(sat)}$. This transistor is ideal for use as a driver in DC/DC converters and actuators.

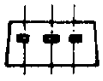
In addition, a small resin-molded insulation type package contributes to high-density mounting and reduction of mounting cost.

FEATURES

- High h_{FE} and low $V_{CE(sat)}$:
  $h_{FE} \geq 100$ ($V_{CE} = -2$ V, $I_C = -1$ A)
  $V_{CE(sat)} \leq 0.3$ V ($I_C = -3$ A, $I_B = -0.15$ A)
- Full-mold package that does not require an insulating board or bushing when mounting.

PACKAGE DRAWING (UNIT: mm)





Electrode Connection
1. Base
2. Collector
3. Emitter

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Collector to base voltage	V_{CBO}	−100	V
Collector to emitter voltage	V_{CEO}	−60	V
Emitter to base voltage	V_{EBO}	−7.0	V
Collector current (DC)	$I_{C(DC)}$	−5.0	A
Collector current (pulse)	$I_{C(pulse)}$*	−10	A
Base current (DC)	$I_{B(DC)}$	−2.5	A
Total power dissipation	P_T (Tc = 25°C)	25	W
Total power dissipation	P_T (Ta = 25°C)	2.0	W
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

* PW ≤ 300 μs, duty cycle ≤ 50%

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ELECTRICAL CHARACTERISTICS (Ta = 25°C)

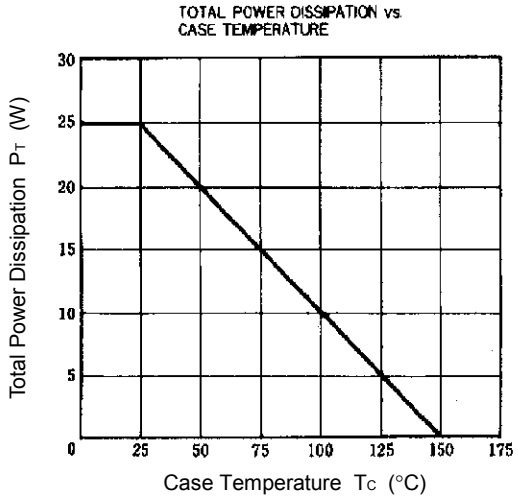
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector to emitter voltage	$V_{CEO(SUS)}$	I_C = –3.0 A, I_B = –0.3 A, L = 1 mH	–60			V
Collector to emitter voltage	$V_{CEX(SUS)}$	I_C = –3.0 A, I_{B1} = –I_{B2} = –0.3 A, $V_{BE(OFF)}$ = 1.5 V, L = 180 μH, clamped	–60			V
Collector cutoff current	I_{CBO}	V_{CB} = –60 V, I_E = 0			–10	μA
Collector cutoff current	I_{CER}	V_{CE} = –60 V, R_{BE} = 50 Ω, Ta = 125°C			–1.0	mA
Collector cutoff current	I_{CEX1}	V_{CE} = –60 V, $V_{BE(OFF)}$ = 1.5 V			–10	μA
Collector cutoff current	I_{CEX2}	V_{CE} = –60 V, $V_{BE(OFF)}$ = 1.5 V, Ta = 125 °C			–1.0	mA
Emitter cutoff current	I_{EBO}	V_{EB} = –5.0 V, I_C = 0			–10	μA
DC current gain	h_{FE1}*	V_{CE} = –2.0 V, I_C = –0.5 A	100			
DC current gain	h_{FE2}*	V_{CE} = –2.0 V, I_C = –1.0 A	100		400	
DC current gain	h_{FE3}*	V_{CE} = –2.0 V, I_C = –3.0 A	60			
Collector saturation voltage	$V_{CE(sat)1}$*	I_C = –3.0 A, I_B = –0.15 A			–0.3	V
Collector saturation voltage	$V_{CE(sat)2}$*	I_C = –4.0 A, I_B = –0.2 A			–0.5	V
Base saturation voltage	$V_{BE(sat)1}$*	I_C = –3.0 A, I_B = –0.15 A			–1.2	V
Base saturation voltage	$V_{BE(sat)2}$*	I_C = –4.0 A, I_B = –0.2 A			–1.5	V
Collector capacitance	C_{ob}	V_{CB} = –10 V, I_E = 0, f = 1.0 MHz		130		pF
Gain bandwidth product	f_T	V_{CE} = –10 V, I_C = –0.5 A		80		MHz
Turn-on time	t_{on}	I_C = –3.0 A, R_L = 17 Ω, I_{B1} = –I_{B2} = –0.15 A, V_{CC} ≅ –50 V Refer to the test circuit.			0.3	μs
Storage time	t_{stg}				1.5	μs
Fall time	t_f				0.3	μs

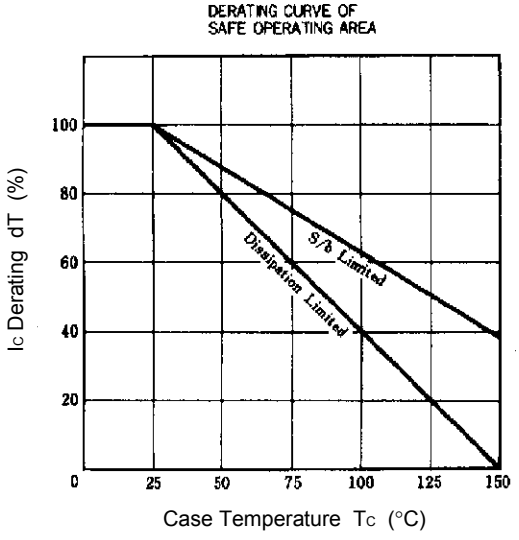
* Pulse test PW ≤ 350 μs, duty cycle ≤ 2%

h_{FE} CLASSIFICATION

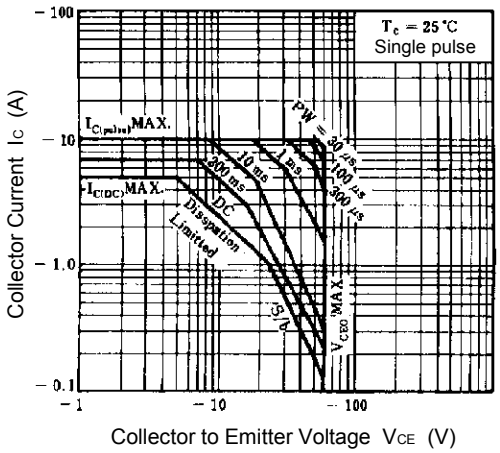
Marking	M	L	K
h_{FE2}	100 to 200	150 to 300	200 to 400

TYPICAL CHARACTERISTICS (Ta = 25°C)

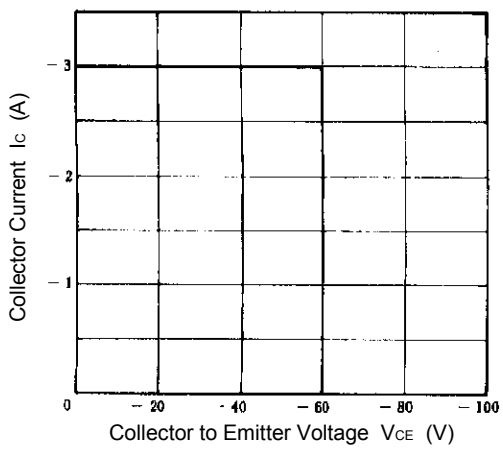




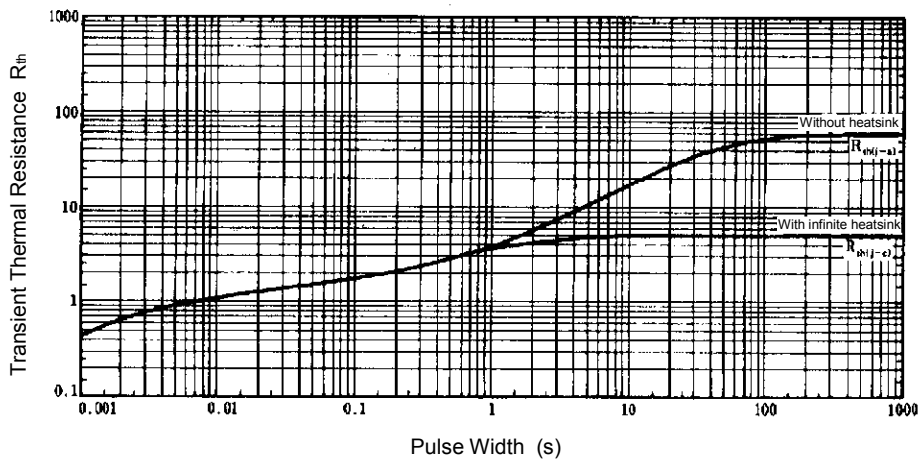
FORWARD BIAS SAFE OPERATING AREA



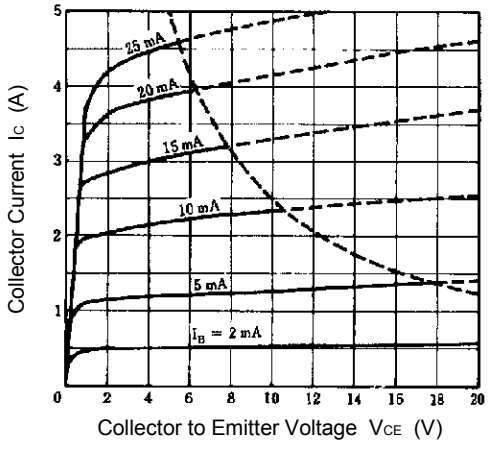
REVERSE BIAS SAFE OPERATING AREA



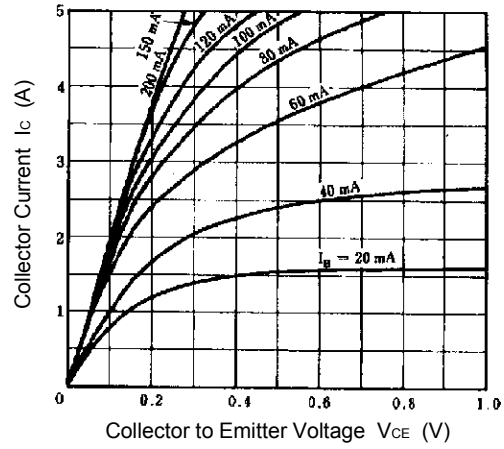
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



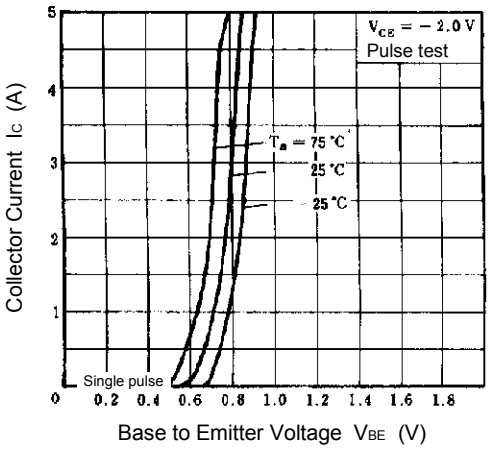
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



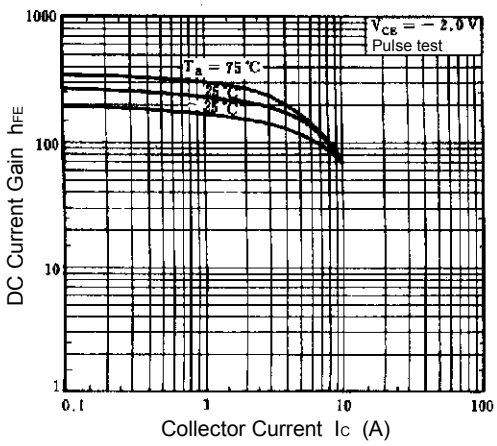
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



COLLECTOR CURRENT vs.
BASE TO EMITTER VOLTAGE

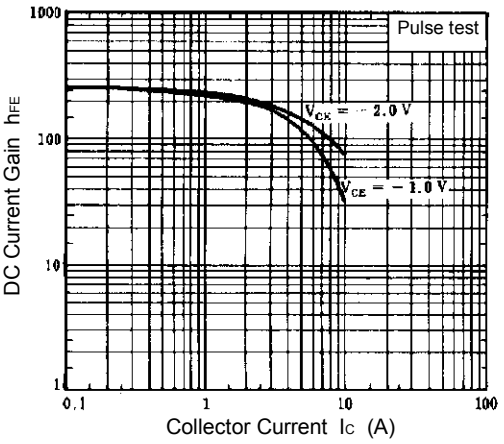


DC CURRENT GAIN vs. COLLECTOR CURRENT

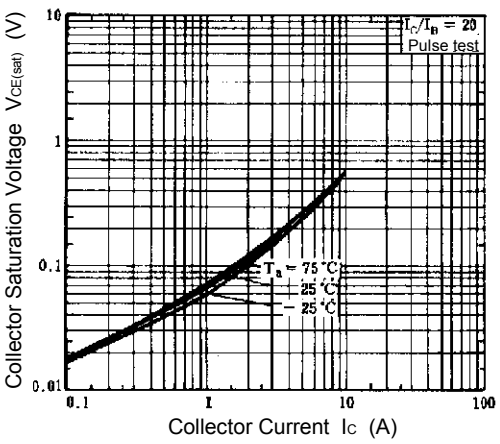


Pulse test

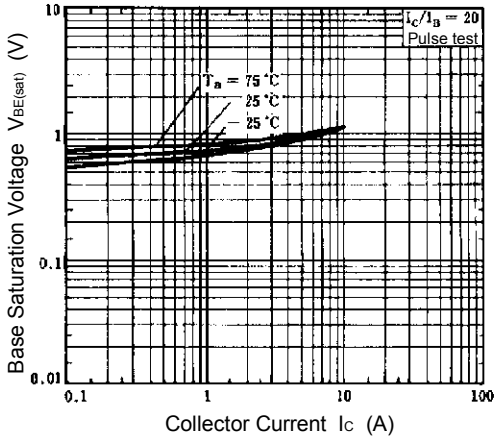
DC CURRENT GAIN vs.COLLECTOR CURRENT



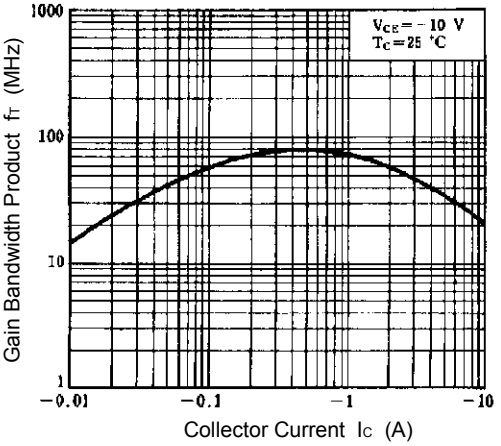
COLLECTOR SATURATION VOLTAGE vs.
COLLECTOR CURRENT

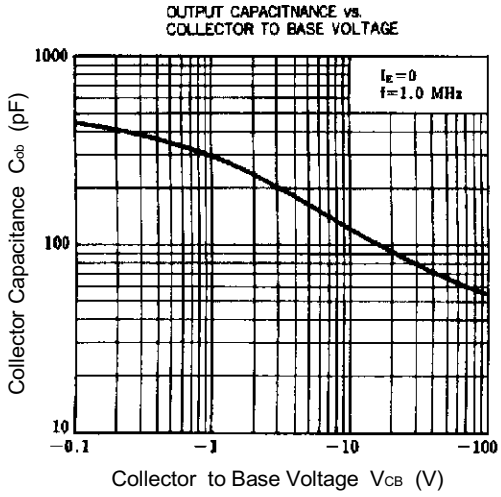


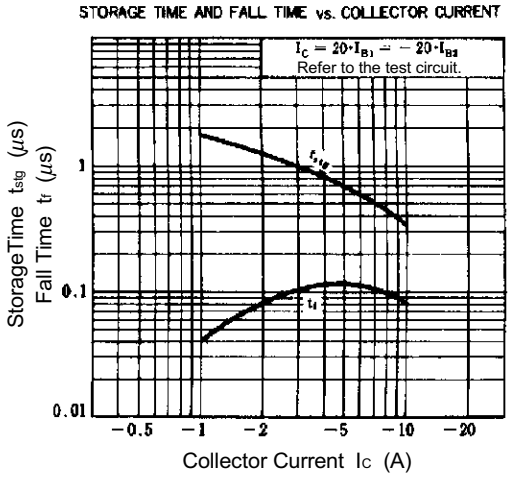
BASE SATURATION VOLTAGE vs.
COLLECTOR CURRENT



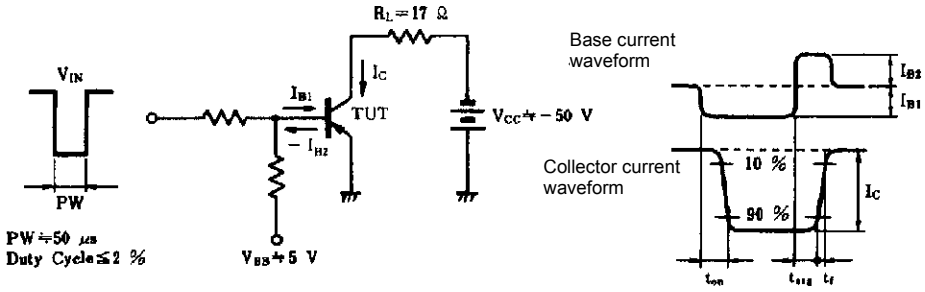
GAIN BANDWIDTH PROUCT vs.
COLLECTOR CURRENT







SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



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