2SA1774

PNP Silicon General Purpose Amplifier Transistor

This PNP transistor is designed for general purpose amplifier applications. This device is housed in the SC−75/SOT−416/SC−90 package which is designed for low power surface mount applications, where board space is at a premium.

Features

- Reduces Board Space
- High h_{FE}, 210−460 (typical)
- Low $V_{CE(sat)}$, < 0.5 V
- Available in 8 mm, 7−inch/3000 Unit Tape and Reel
- Pb−Free Packages are Available*

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	$V_{(BR)CBO}$	−60	Vdc
Collector − Base Voltage	$V_{(BR)CEO}$	−50	Vdc
Emitter − Base Voltage	$V_{(BR)EBO}$	−6.0	Vdc
Collector Current − Continuous	I_C	−100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation (Note 1)	P_D	150	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 ~ +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Device mounted on a FR−4 glass epoxy printed circuit board using the minimum recommended footprint.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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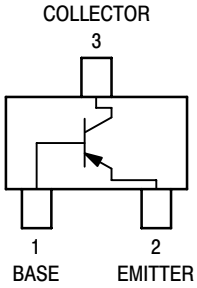
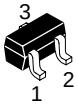
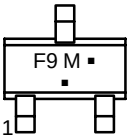




SC−75
CASE 463−01
STYLE 1

MARKING DIAGRAM



F9 = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector−Base Breakdown Voltage (I_C = −50 μAdc, I_E = 0)	$V_{(BR)CBO}$	−60	−	−	Vdc
Collector−Emitter Breakdown Voltage (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−50	−	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −50 μAdc, I_E = 0)	$V_{(BR)EBO}$	−6.0	−	−	Vdc
Collector−Base Cutoff Current (V_{CB} = −30 Vdc, I_E = 0)	I_{CBO}	−	−	−0.5	nA
Emitter−Base Cutoff Current (V_{EB} = −5.0 Vdc, I_B = 0)	I_{EBO}	−	−	−0.5	μA
Collector−Emitter Saturation Voltage (Note 2) (I_C = −50 mAdc, I_B = −5.0 mAdc)	$V_{CE(sat)}$	−	−	−0.5	Vdc
DC Current Gain (Note 2) (V_{CE} = −6.0 Vdc, I_C = −1.0 mAdc)	h_{FE}	120	−	560	−
Transition Frequency (V_{CE} = −12 Vdc, I_C = −2.0 mAdc, f = 30 MHz)	f_T	−	140	−	MHz
Output Capacitance (V_{CB} = −12 Vdc, I_E = 0 Adc, f = 1 MHz)	C_{OB}	−	3.5	−	pF

2. Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

ORDERING INFORMATION

Device	Package	Shipping†
2SA1774	SC−75	3000 / Tape & Reel
2SA1774G	SC−75 (Pb−Free)	3000 / Tape & Reel
2SA1774T1	SC−75	3000 / Tape & Reel
2SA1774T1G	SC−75 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL ELECTRICAL CHARACTERISTICS

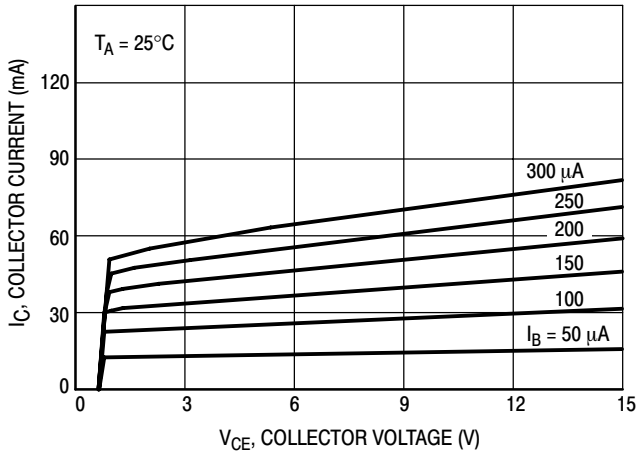


Figure 1. $I_C - V_{CE}$

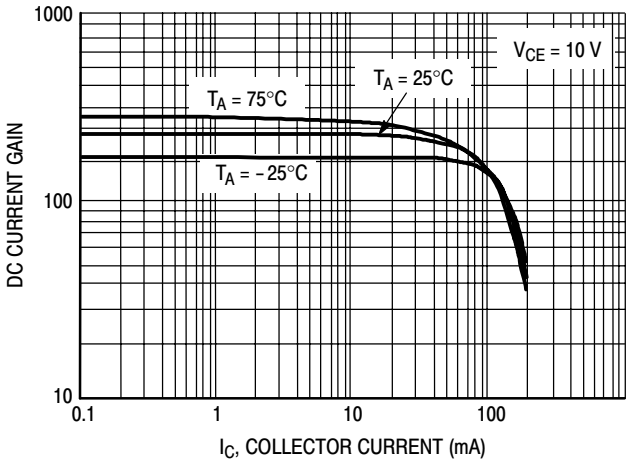


Figure 2. DC Current Gain

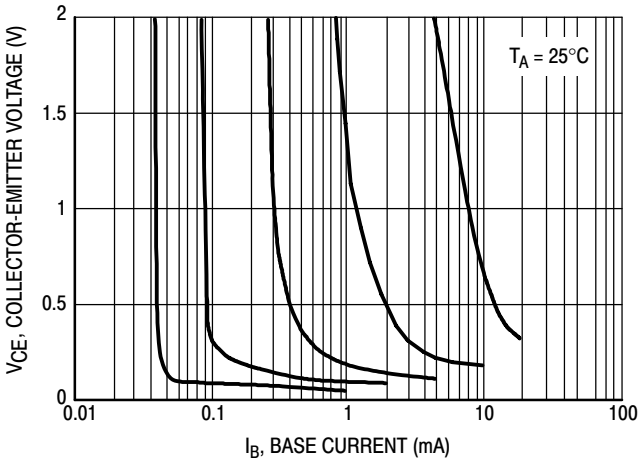


Figure 3. Collector Saturation Region

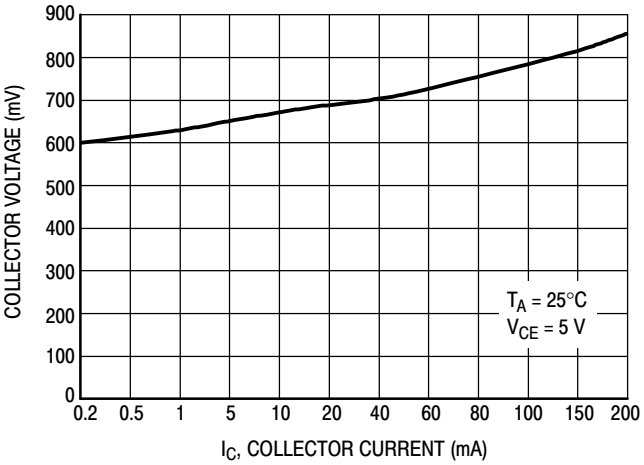


Figure 4. On Voltage

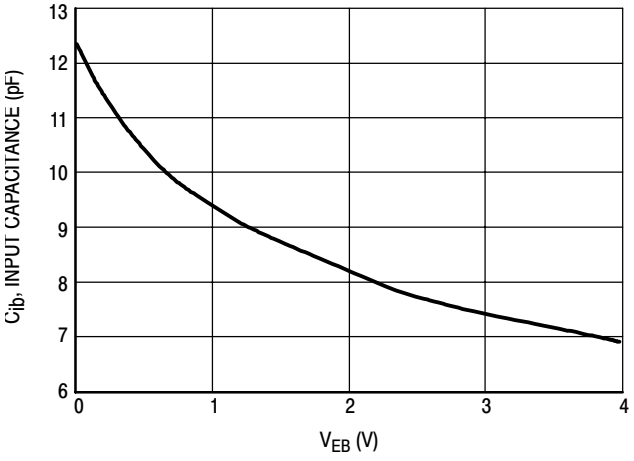


Figure 5. Capacitance

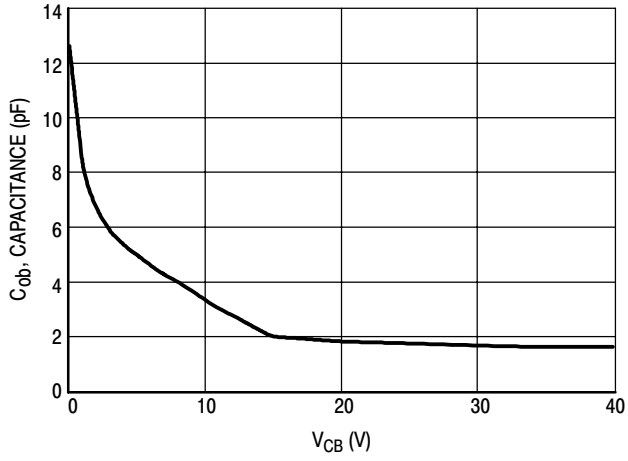
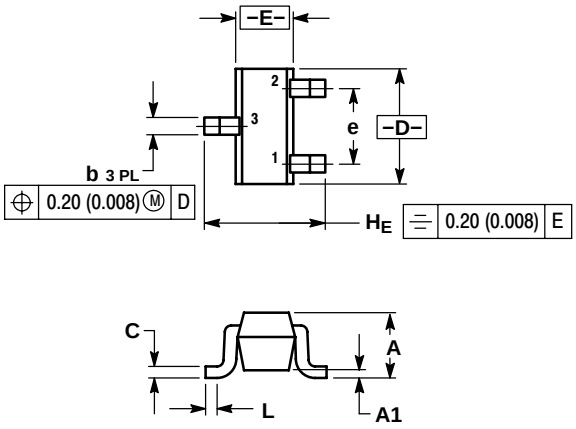


Figure 6. Capacitance

2SA1774

PACKAGE DIMENSIONS

SC−75/SOT−416
CASE 463−01
ISSUE F

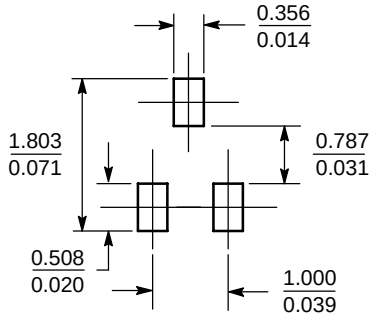


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.15	0.20	0.30	0.006	0.008	0.012
C	0.10	0.15	0.25	0.004	0.006	0.010
D	1.55	1.60	1.65	0.059	0.063	0.067
E	0.70	0.80	0.90	0.027	0.031	0.035
e	1.00 BSC			0.04 BSC		
L	0.10	0.15	0.20	0.004	0.006	0.008
H_E	1.50	1.60	1.70	0.061	0.063	0.065

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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