

Silicon PNP Power Transistors

2SB1343

DESCRIPTION

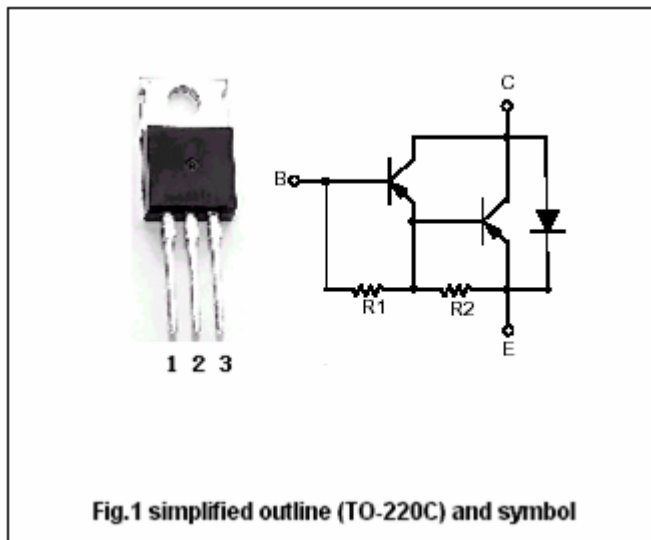
- With TO-220C package
- High DC current gain
- Low saturation voltage
- DARLINGTON

APPLICATIONS

- For low frequency power amplifier and power driver applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter



Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-100	V
V _{CEO}	Collector -emitter voltage	Open base	-100	V
V _{EBO}	Emitter-base voltage	Open collector	-7	V
I _C	Collector current		-8	A
I _{CM}	Collector current-peak		-10	A
P _C	Collector power dissipation	T _a =25°C	2	W
		T _C =25°C	40	
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-5mA; I _B =0	-100			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-50μA; I _E =0	-100			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-3A; I _B =-6mA		-1.0	-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-100V; I _E =0			-10	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-3.0	mA
h _{FE}	DC current gain	I _C =-2A; V _{CE} =-3V	1000		20000	
f _T	Transition frequency	I _C =-0.5A; V _{CE} =-5V		12		MHz
C _{OB}	Output capacitance	I _E =0; V _{CB} =-10V; f=1MHz		90		pF

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PACKAGE OUTLINE

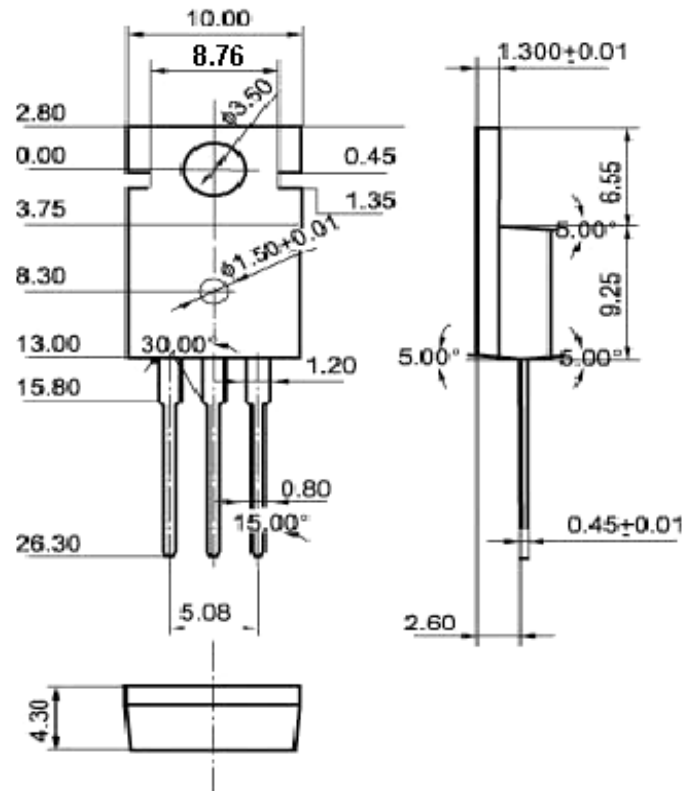


Fig.2 Outline dimensions (unindicated tolerance: ± 0.10 mm)