Silicon PNP Power Transistors 2SB558

DESCRIPTION
·With TO-3 package
·High power dissipation

APPLICATIONS
·For power switching and general purpose applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

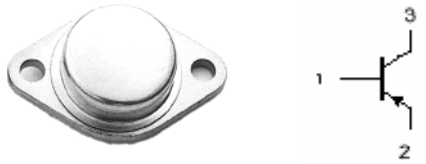

Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-100	V
V_{CEO}	Collector-emitter voltage	Open base	-100	V
V_{EBO}	Emitter-base voltage	Open collector	-6	V
I_C	Collector current		-7	A
P_C	Collector power dissipation	T_C=25□	60	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-65~150	□

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CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=-50mA ;I_B=0	-100			V
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C=-1mA ;I_E=0	-100			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=-1mA ;I_C=0	-6			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-3A; I_B=-0.3A			-1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=-100V; I_E=0			-0.1	mA
I_{EBO}	Emitter cut-off current	V_{EB}=-6V; I_C=0			-0.1	mA
h_{FE}	DC current gain	I_C=-1A ; V_{CE}=-5V	40		140	
f_T	Transition frequency	I_C=-1A ; V_{CE}=-5V		7		MHz

◆ **h_{FE} Classifications**

R	O
40-80	70-140

PACKAGE OUTLINE

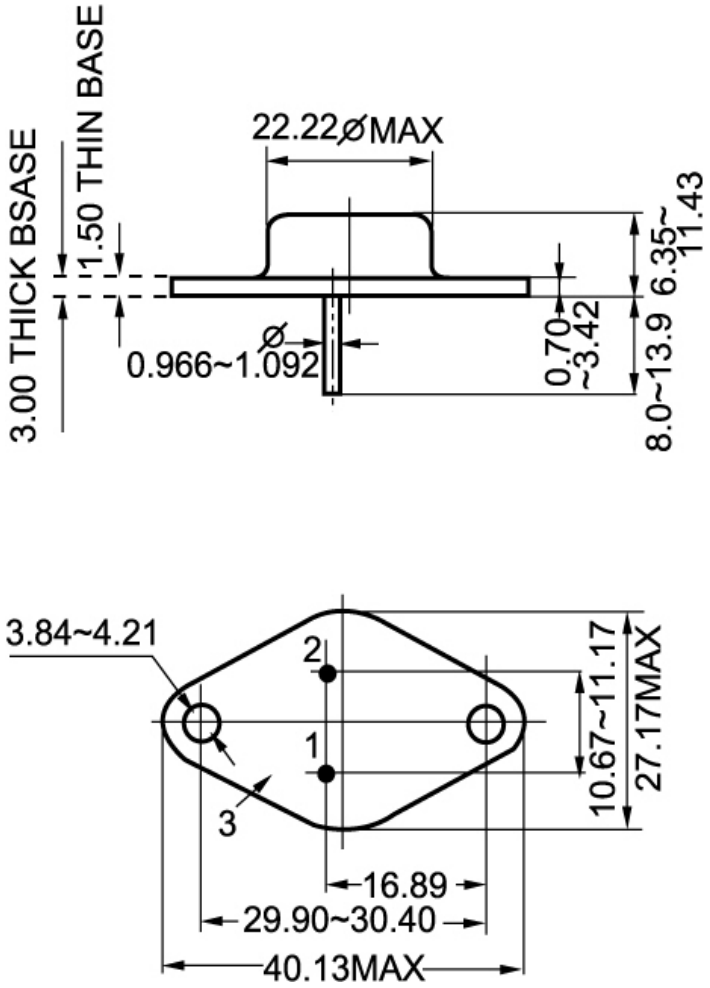

Fig.2 outline dimensions (unindicated tolerance:±0.1mm)