

SILICON POWER TRANSISTOR 2SB768

PNP SILICON TRIPLE DIFFUSED TRANSISTOR

DESCRIPTION

The 2SB768 is designed for Color TV Vertical Deflection Output, especially in Hybrid Integrated Circuits.

FEATURES

- High Voltage: VCEO = -150 V
- Complement to 2SD1033

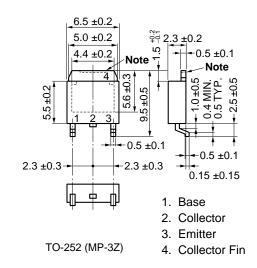
ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Collector to Base Voltage	Vсво	-200	V
Collector to Emitter Voltage	Vceo	-150	V
Emitter to Base Voltage	Vево	-5	V
Collector Current (DC)	IC(DC)	-2	А
Collector Current (pulse) Note 1	C(pulse)	-3	А
Total Power Dissipation (T_A = $25^{\circ}C$) ^{Note 2}	Рт	2.0	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Notes 1. PW \leq 10 ms, Duty Cycle \leq 50%

2. When mounted on ceramic substrate of 7.5 $\text{cm}^2 \times 0.7$ mm

<R> PACKAGE DRAWING (Unit: mm)



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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The mark <R> shows major revised points.

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The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

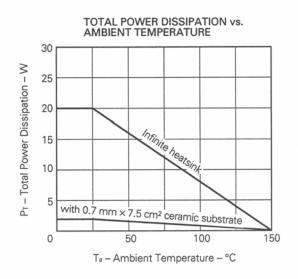
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Cutoff Current	Ісво			-50	μA	$V_{CB} = -150 V$, $I_E = 0$
Emitter Cutoff Current	Іево	1. 		-50	μA	$V_{EB} = -4.0 V, Ic = 0$
DC Current Gain	hfe1***	40	80	200		$V_{CE} = -10 V, I_{C} = -0.4 A$
Collector Saturation Voltage	VcE(sat)***		-0.15	-1.0	V	lc = -500 mA, lb = -50 mA
Gain Badnwidth Product	fr		10		MHz	$V_{CE} = -10 V$, $I_E = -0.4 mA$

*** Pulsed: PW \leq 350 μ s, Duty Cycle \leq 2 %

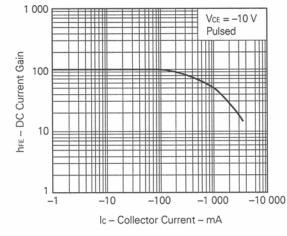
hre Classification

MARKING	М	L	К
hfe1	40 to 80	60 to 120	100 to 200

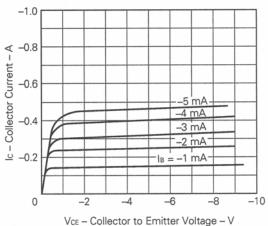
TYPICAL CHARACTERISTICS (Ta = 25 °C)



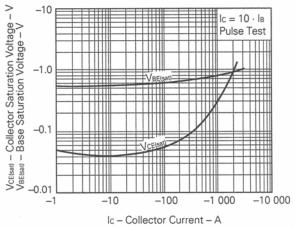


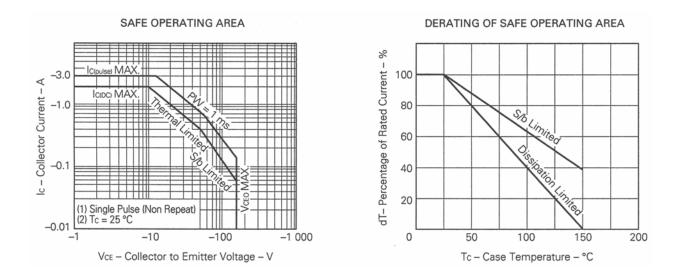


COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT





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