

SANYO

No.2103A

2SA1509/2SC3899

PNP/NPN Epitaxial Planar Silicon Transistors

Switching Applications
(with Bias Resistance)**Applications**

- Switching circuits, inverter circuits, interface circuits, driver circuits

Features

- On-chip bias resistance: $R_1 = 47k\Omega$
- Small-sized package: SPA

(): 2SA1509

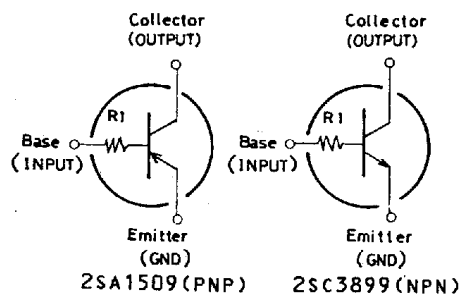
Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

			unit
Collector to Base Voltage	V_{CB0}	(-) 50	V
Collector to Emitter Voltage	V_{CEO}	(-) 50	V
Emitter to Base Voltage	V_{EBO}	(-) 5	V
Collector Current	I_C	(-) 100	mA
Collector Current (Pulse)	I_{CP}	(-) 200	mA
Collector Dissipation	P_C	300	mW
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

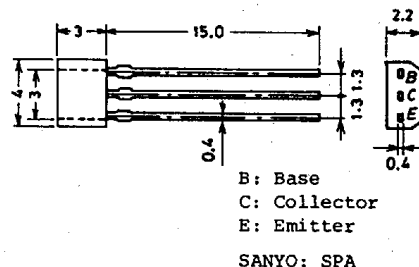
Electrical Characteristics at $T_a = 25^\circ\text{C}$

			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	$V_{CB} = (-) 40\text{V}, I_E = 0$			(-) 0.1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = (-) 5\text{V}, I_C = 0$			(-) 0.1	μA
DC Current Gain	h_{FE}	$V_{CE} = (-) 5\text{V}, I_C = (-) 10\text{mA}$	100			
Gain-Bandwidth Product	f_T	$V_{CE} = (-) 10\text{V}, I_C = (-) 5\text{mA}$		250		MHz
				(200)		MHz
Output Capacitance	c_{ob}	$V_{CB} = (-) 10\text{V}, f = 1\text{MHz}$		3.7		pF
				(5.5)		pF
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = (-) 5\text{mA}, I_E = (-) 0.25\text{mA}$		(-) 0.1	(-) 0.3	V
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = (-) 10\mu\text{A}, I_E = 0$	(-) 50			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = (-) 100\mu\text{A}, R_{BE} = \infty$	(-) 50			V

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Electrical Connection**Case Outline 2033**

(unit:mm)



Specifications and information herein are subject to change without notice.

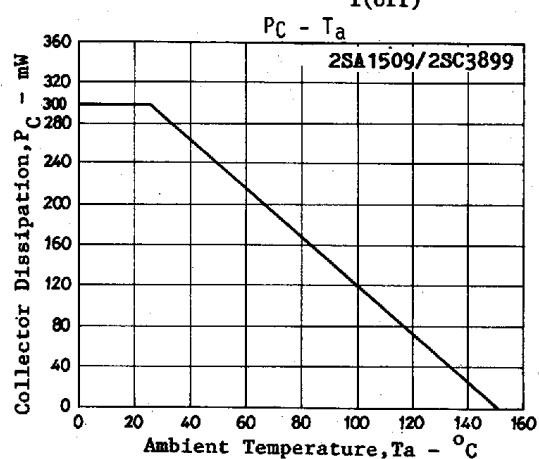
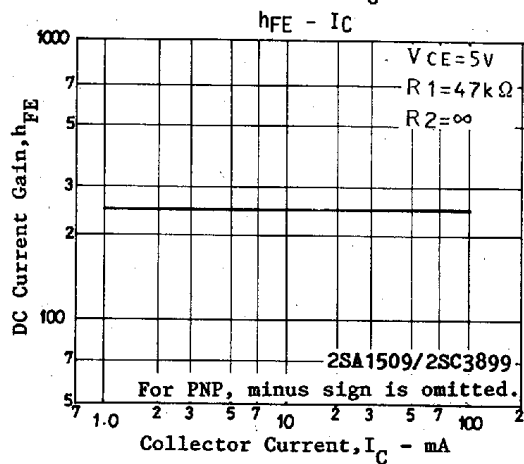
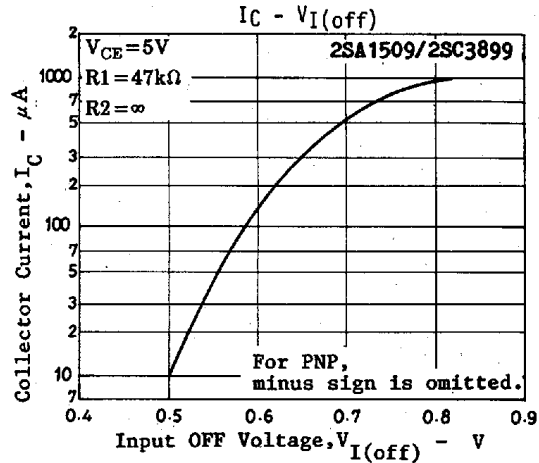
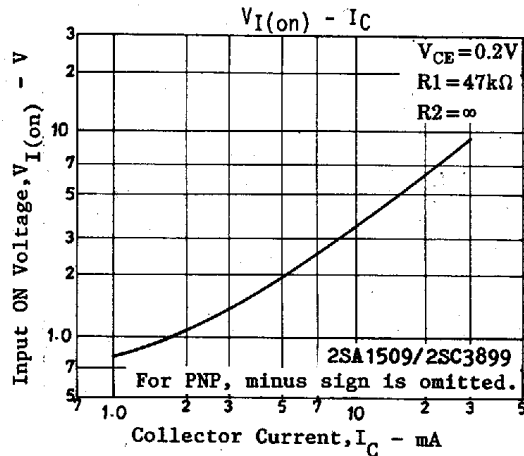
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3307KI/8046AT, TS No. 2103-1/2

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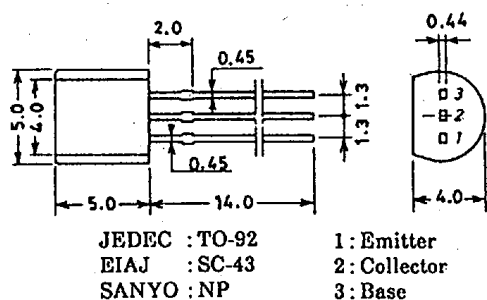
			min	typ	max	unit
Input OFF-State Voltage	$V_{I(off)}$	$V_{CE}=(-)5V,$ $I_{CE}=(-)100\mu A$	$(-)0.4$	$(-)0.55$	$(-)0.8$	V
Input ON-State Voltage	$V_{I(on)}$	$V_{CE}=(-)0.2V,$ $I_C=5mA$	$(-)0.8$	$(-)2.0$	$(-)4.0$	V
Input Resistance	R_I		33	47	61	k Ω



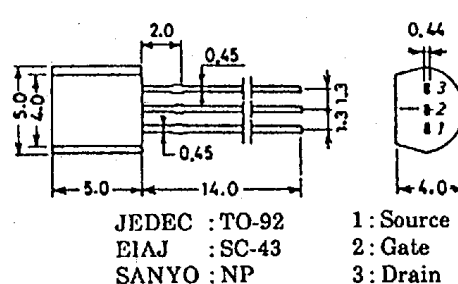
CASE OUTLINES OF LEAD FORMED SMALL SIGNAL TRANSISTORS

- All of Sanyo lead formed small signal transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

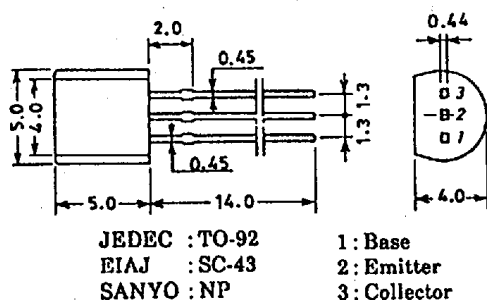
Case Outline 2003A/2003B (unit : mm)



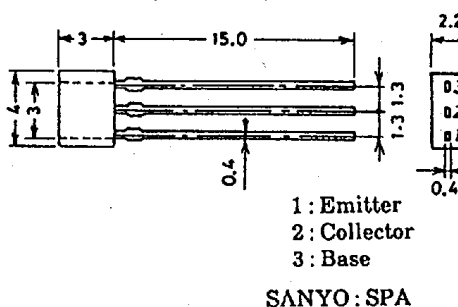
Case Outline 2019A/2019B (unit : mm)



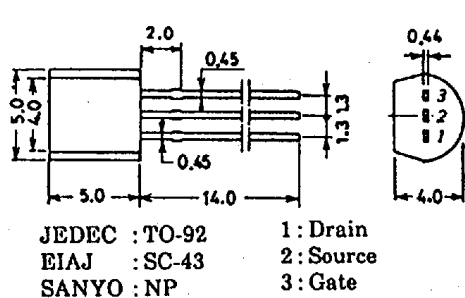
Case Outline 2004A (unit : mm)



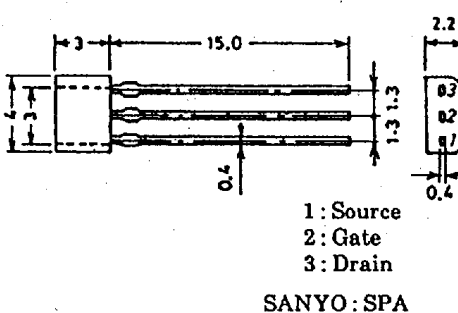
Case Outline 2033 (unit : mm)



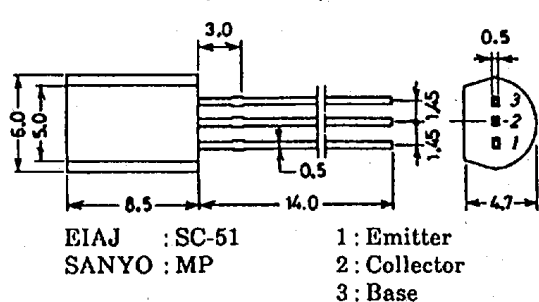
Case Outline 2005A (unit : mm)



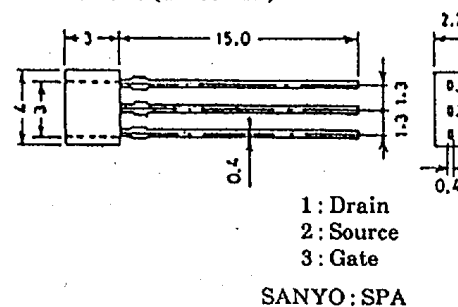
Case Outline 2034/2034A (unit : mm)



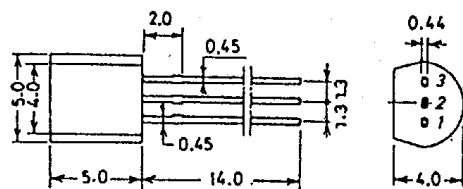
Case Outline 2006A (unit : mm)



Case Outline 2040 (unit : mm)



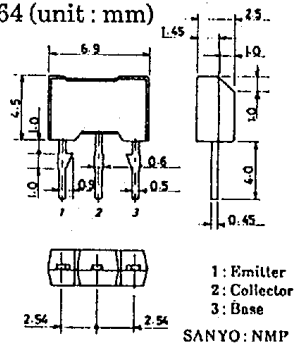
Case Outline 2061 (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1: Emitter
2: Base
3: Collector

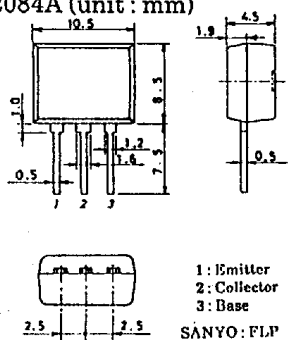
Case Outline 2064 (unit : mm)



1: Emitter
2: Collector
3: Base

SANYO: NMP

Case Outline 2084A (unit : mm)



1: Emitter
2: Collector
3: Base

SANYO: FLP