NPN Triple Diffused Planar Silicon Transistor

2SC5823

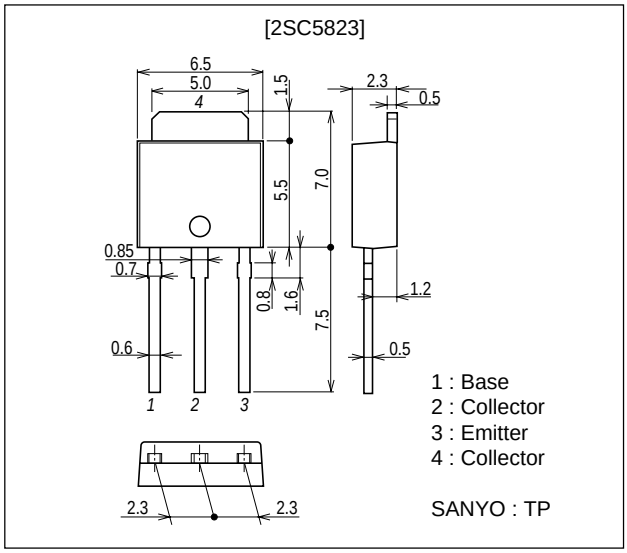
Switching Regulator Applications

Features

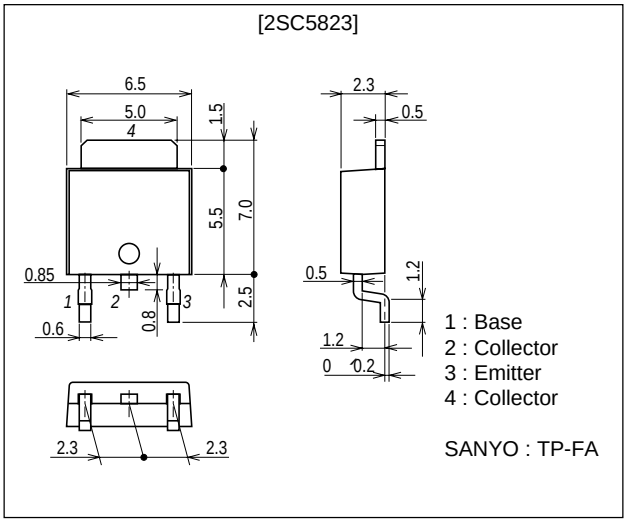
- High breakdown voltage.
- High-speed switching.
- Wide ASO.
- Adoption of MBIT process.

Package Dimensions

unit : mm
2045B



unit : mm
2044B



Specifications

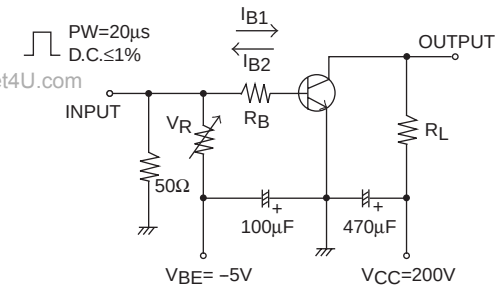
Absolute Maximum Ratings at Ta=25°C

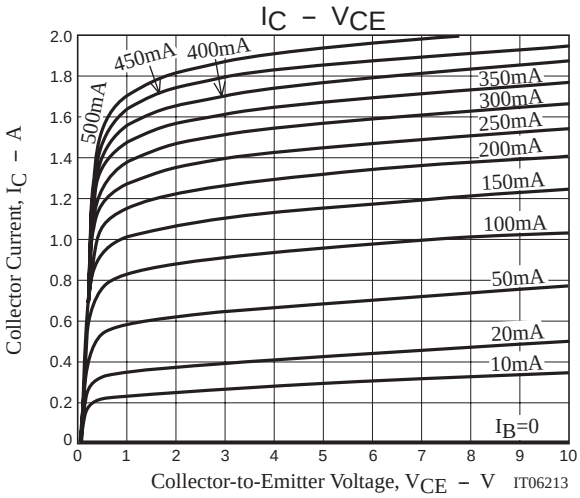
Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		700	V
Collector-to-Emitter Voltage	V_{CEO}		400	V
Emitter-to-Base Voltage	V_{EBO}		8	V
Collector Current	I_C		1.5	A
Collector Current (Pulse)	I_{CP}	PW≤300μs, duty cycle≤10%	3	A
Base Current	I_B		0.7	A
Collector Dissipation	P_C		1.0	W
		Tc=25°C	10	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		−55 to +150	°C

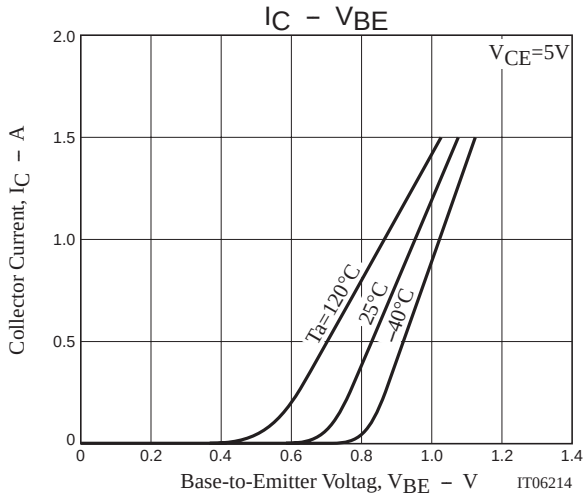
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=400V, I_E=0			10	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=5V, I_C=0			10	μA
DC Current Gain	$h_{FE}1$	V_{CE}=5V, I_C=0.1A	20		50	
	$h_{FE}2$	V_{CE}=5V, I_C=0.7A	10			
	$h_{FE}3$	V_{CE}=5V, I_C=1mA	10			
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=0.1A		20		MHz
Output Capacitance	Cob	V_{CB}=10V, f=1MHz		10		pF
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C=0.7A, I_B=0.14A			0.8	V
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=0.7A, I_B=0.14A			1.5	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=1mA, I_E=0	700			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=5mA, R_{BE}=∞	400			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=1mA, I_C=0	8			V
Turn-On Time	t_{on}	I_C=1A, I_{B1}=0.2A, I_{B2}=-0.4A,R_L=200Ω, V_{CC}=200V			0.5	μs
Storage Time	t_{stg}	I_C=1A, I_{B1}=0.2A, I_{B2}=-0.4A,R_L=200Ω, V_{CC}=200V			2.5	μs
Fall Time	t_f	I_C=1A, I_{B1}=0.2A, I_{B2}=-0.4A,R_L=200Ω, V_{CC}=200V			0.25	μs

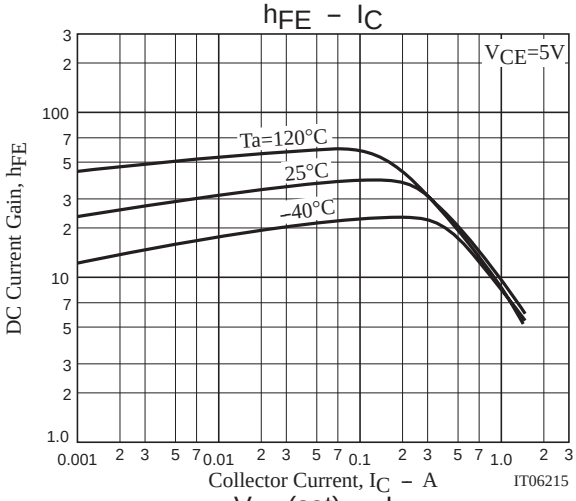
Switching Time Test Circuit



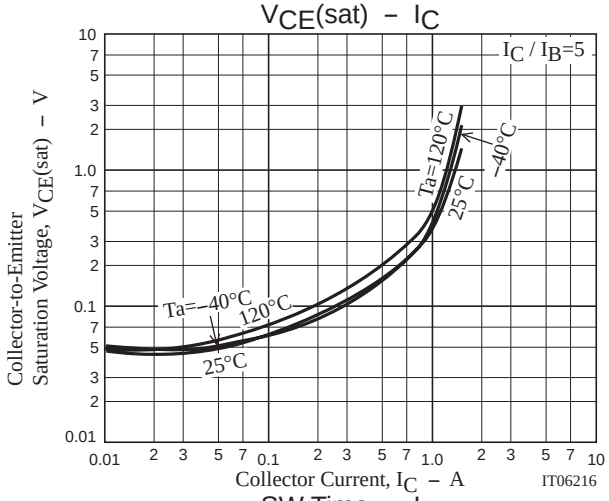




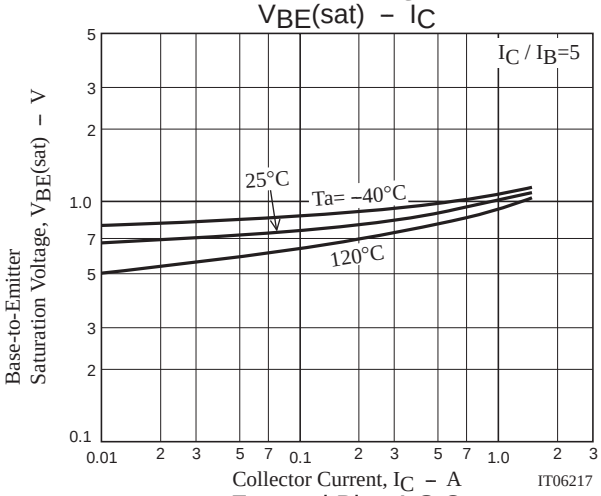
h_{FE} – I_C



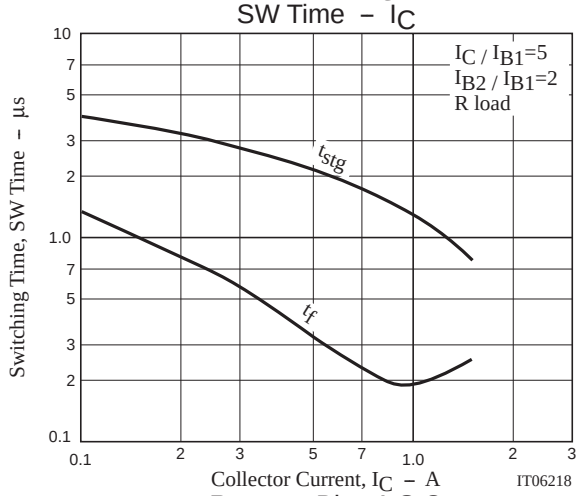
$V_{CE}(sat)$ – I_C



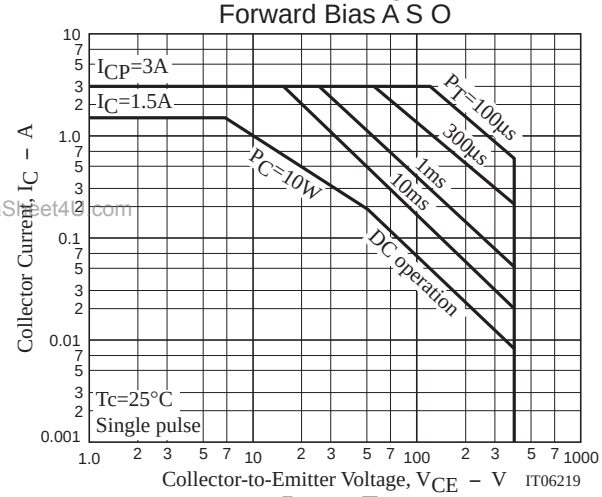
$V_{BE}(sat)$ – I_C



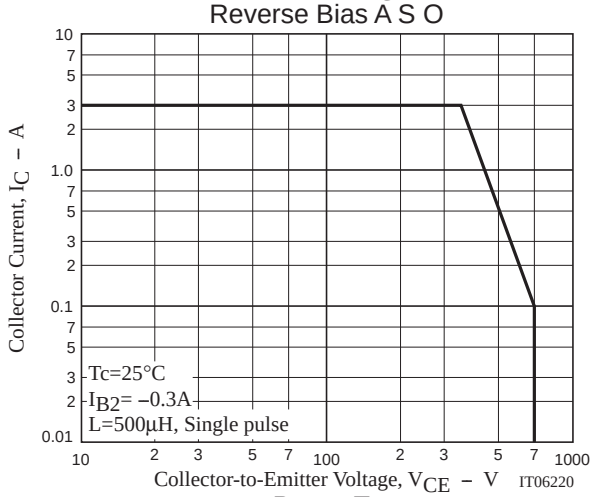
SW Time – I_C



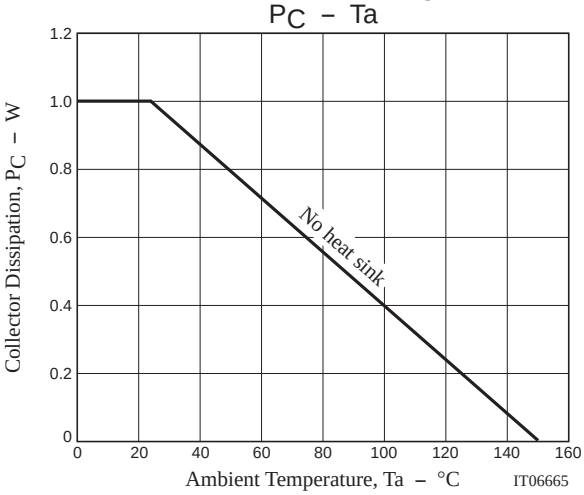
Forward Bias A S O



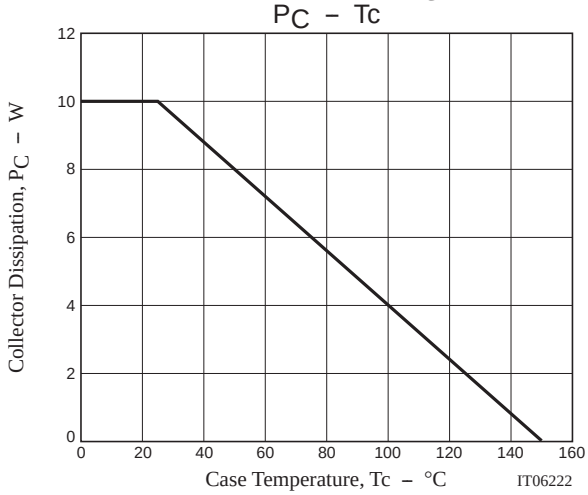
Reverse Bias A S O



P_C – Ta



P_C – Tc



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