

DARLINGTON POWER TRANSISTOR 2SD1843

NPN SILICON EPITAXIAL TRANSISTOR (DARLINGTON CONNECTION) FOR LOW-FREQUENCY POWER AMPLIFIERS AND LOW-SPEED SWITCHING

The 2SD1843 is a Darlington connection transistor with on-chip dumper diode in collector to emitter and zener diode in collector to base. This transistor is ideal for use in acuator drives such as motors, relays, and solenoids.

FEATURES

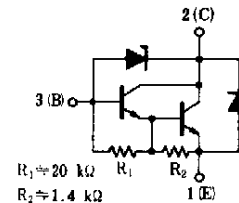
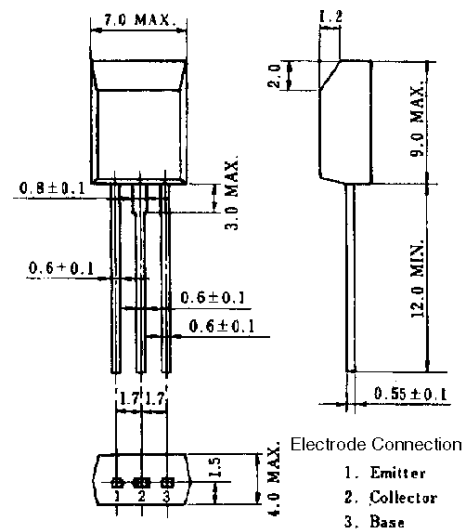
- High DC current gain due to Darlington connection
- High surge resistance due to on-chip protection elements:
C to E: Dumper diode
C to B: Zener diode
- Low collector saturation voltage

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Collector to base voltage	V _{CB0}	60±10	V
Collector to emitter voltage	V _{CEO}	60±10	V
Emitter to base voltage	V _{EBO}	7.0	V
Collector current (DC)	I _{C(DC)}	±1.0	A
Collector current (pulse)	I _{C(pulse)*}	±2.0	A
Total power dissipation	P _{T(Ta=25°C)}	1.0	W
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

* PW ≤ 10 ms, duty cycle ≤ 50%

PACKAGE DRAWING (UNIT: mm)



ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector cutoff current	I _{CBO}	V _{CB} = 40 V, I _E = 0			0.5	μA
Emitter cutoff current	I _{EBO}	V _{EB} = 5.0 V, I _C = 0			1.0	mA
DC current gain	h _{FE2} **	V _{CE} = 2.0 V, I _C = 0.2 A	1000			
DC current gain	h _{FE2} **	V _{CE} = 2.0 V, I _C = 0.5 A	2000		30000	
Collector saturation voltage	V _{CE(sat)**}	I _C = 0.5 A, I _B = 0.5 mA			1.5	V
Base saturation voltage	V _{BE(sat)**}	I _C = 0.5 A, I _B = 0.5 mA			2.0	V
Turn-on time	t _{ON}	I _C = 0.5 A, R _L = 100 Ω		0.5		μs
Storage time	t _{stg}	I _{B1} = -I _{B2} = 0.1 mA, V _{CC} = 50 V		1.0		μs
Fall time	t _f			1.0		μs

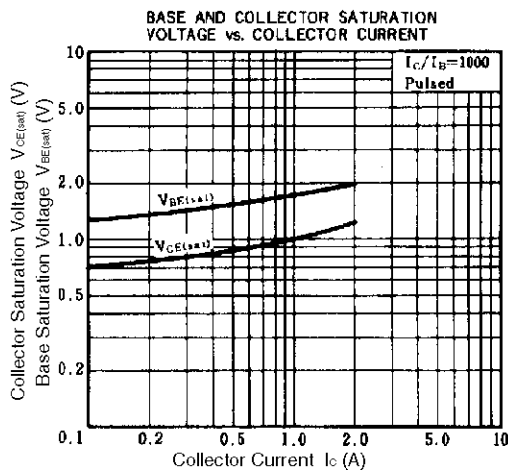
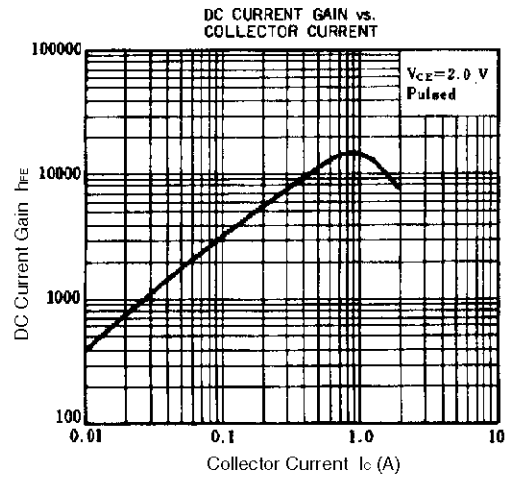
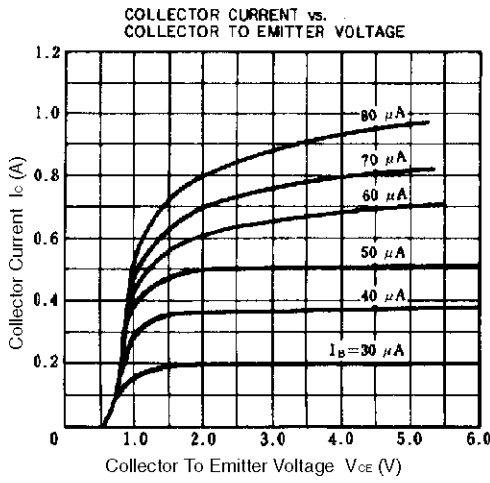
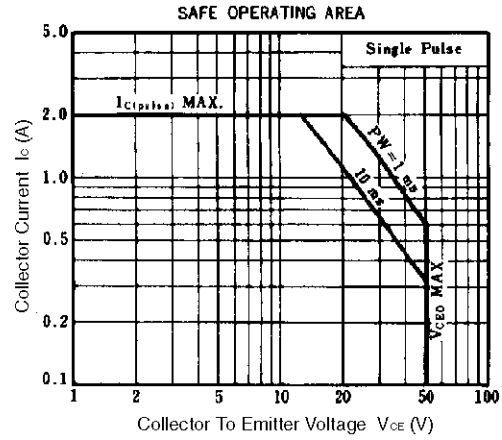
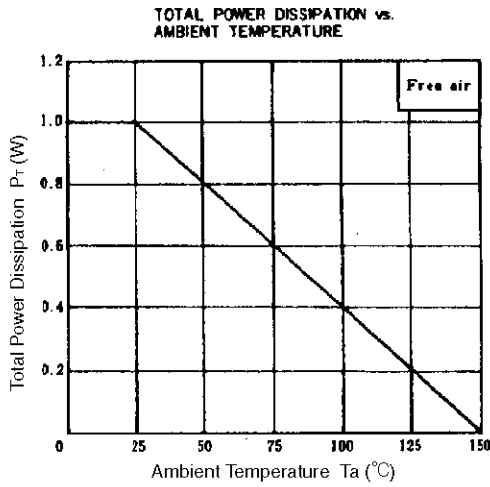
** Pulse test PW ≤ 350 μs, duty cycle ≤ 2%

h_{FE} CLASSIFICATION

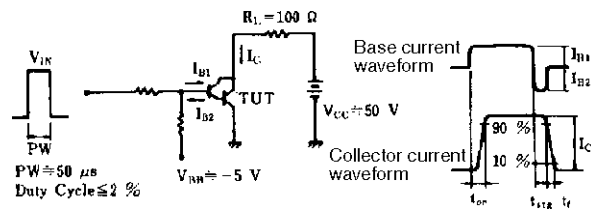
Marking	M	L	K
h _{FE2}	2000 to 5000	4000 to 10000	8000 to 30000

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TYPICAL CHARACTERISTICS (Ta = 25°C)



SWITCHING TIME (t_{on} , t_{stg} , t_f) TEST CIRCUIT



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