

Silicon NPN Power Transistors

2SD725

DESCRIPTION

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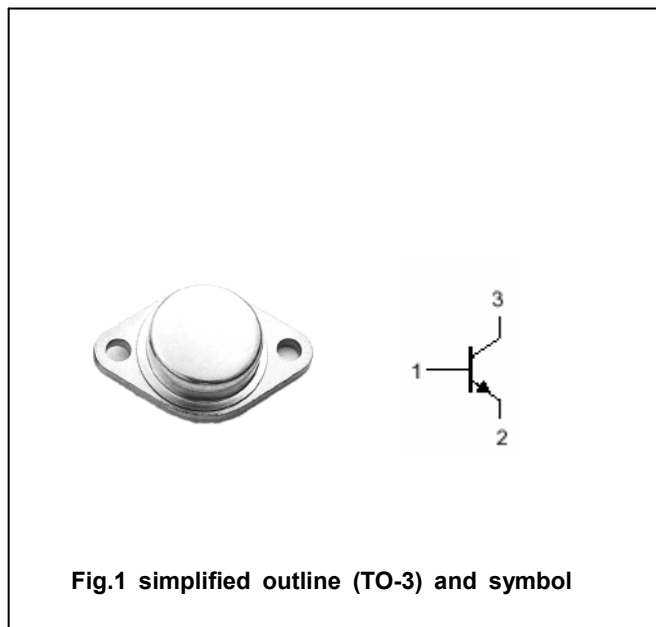
- With TO-3 package
- High voltage ,high speed
- Low collector saturation voltage

APPLICATIONS

- For high voltage,power switching and TV horizontal output applications

PINNING(see fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	600	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		7	A
P_C	Collector power dissipation	$T_C = 25 \square$	50	W
T_j	Junction temperature		150	$\square$
T_{stg}	Storage temperature		-65~150	$\square$

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CHARACTERISTICS

Tj=25°C unless otherwise specified

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	$I_C=0.1A; I_B=0$	600			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	$I_E=1mA; I_C=0$	5			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=5A; I_B=1A$			5.0	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=5A; I_B=1A$			1.5	V
I_{CBO}	Collector cut-off current	$V_{CB}=800V; I_E=0$			10	μA
I_{EBO}	Emitter cut-off current	$V_{EB}=5V; I_C=0$			0.1	mA
h_{FE-1}	DC current gain	$I_C=1A; V_{CE}=5V$	8		36	
h_{FE-2}	DC current gain	$I_C=5A; V_{CE}=5V$	5			

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PACKAGE OUTLINE

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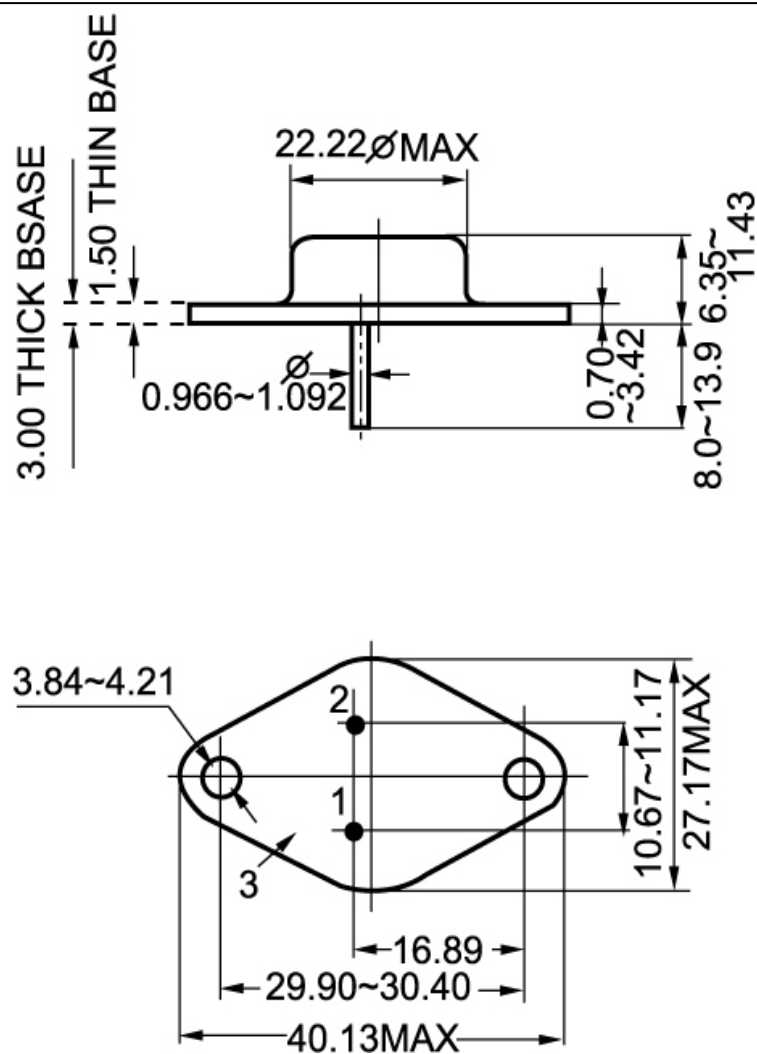


Fig.2 Outline dimensions