

Silicon NPN Power Transistors

2SD950

DESCRIPTION

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- With TO-3 package
- Built-in damper diode
- High voltage capability

APPLICATIONS

- Line-operated horizontal deflection output applications

PINNING(see fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

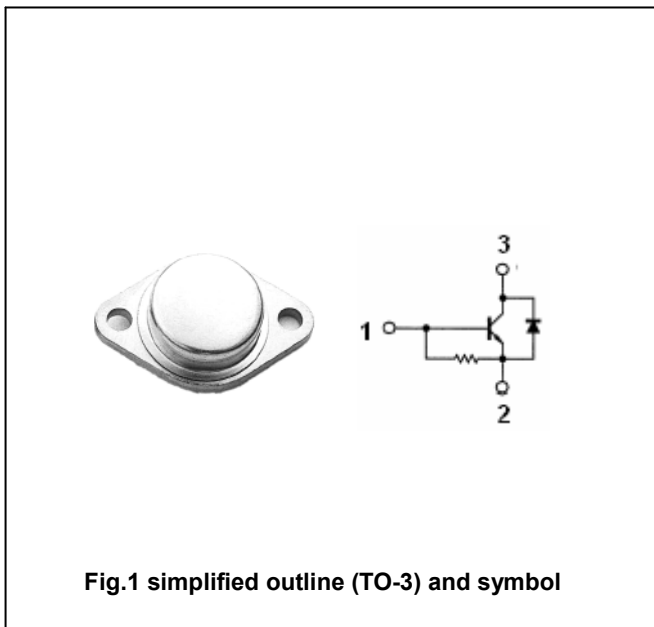


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		3	A
I_{CM}	Collector current-peak		4.5	A
P_T	Total power dissipation	$T_C = 25\square$	42	W
T_j	Junction temperature		130	$\square$
T_{stg}	Storage temperature		-65~130	$\square$

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CHARACTERISTICS

T_j=25°C unless otherwise specified

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =500mA; I _C =0	5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =2A; I _B =0.75A			5.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =2A; I _B =0.75A			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =750V; I _E =0			50	μA
		V _{CB} =1500V; I _E =0			1.0	mA
h _{FE-1}	DC current gain	I _C =1A; V _{CE} =5V	8			
h _{FE-2}	DC current gain	I _C =2A; V _{CE} =10V	3			
V _F	Diode forward voltage	I _F =4A			1.7	V
t _f	Fall time	I _C =2A; I _{Bend} =0.75A; L _B =10μH			0.9	μs
t _s	Storage time			11		μs

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PACKAGE OUTLINE

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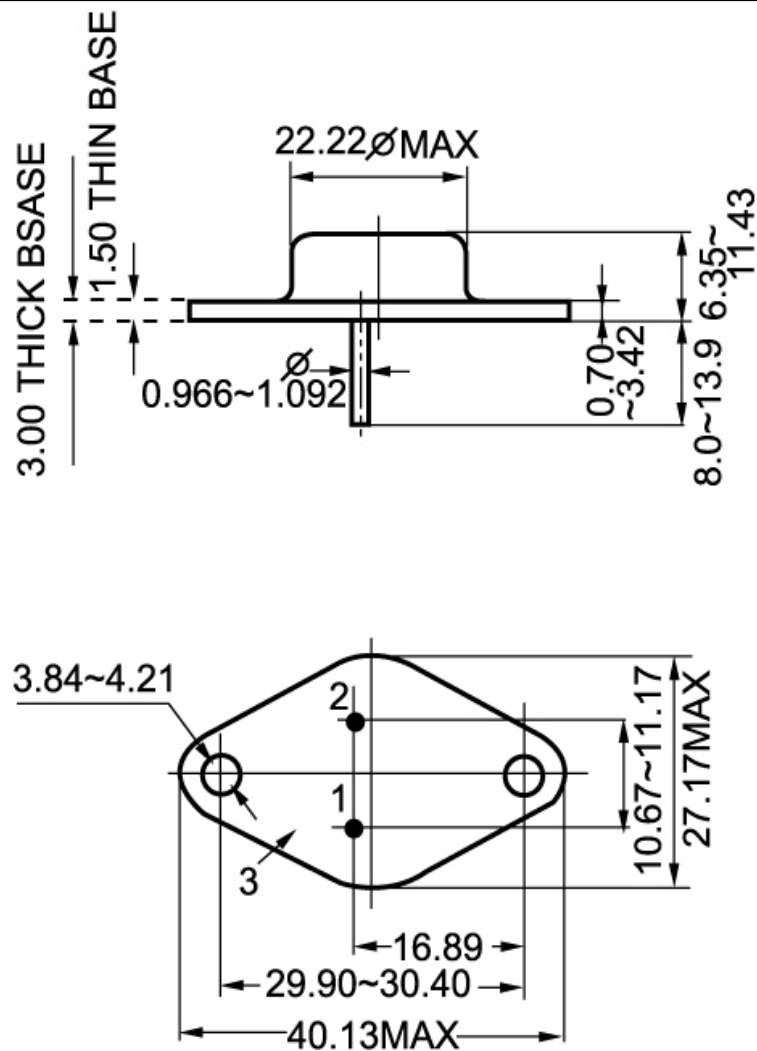


Fig.2 Outline dimensions