

# MOS FIELD EFFECT POWER TRANSISTORS 2SJ133, 2SJ133-Z

### P-CHANNEL POWER MOS FET FOR SWITCHING

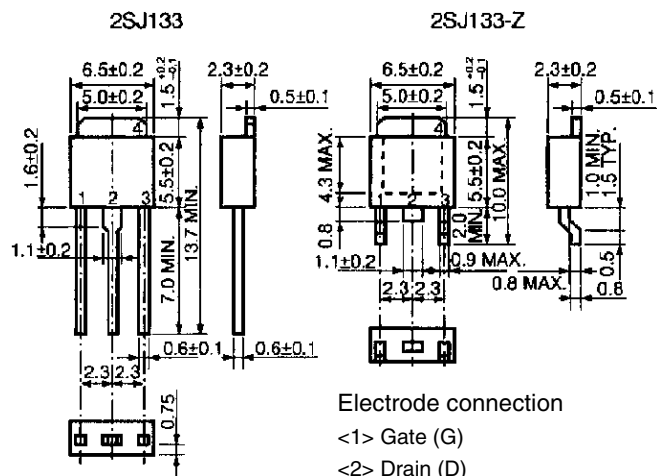
#### FEATURES

- Gate drive available at logic level ( $V_{GS} = -4\text{ V}$ )
- High current control available in small dimension due to low  $R_{DS(on)} (\cong 0.45\ \Omega)$
- 2SJ133-Z is a lead process product and is deal for mounting a hybrid IC.

#### QUALITY GRADES

- Standard  
Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

#### PACKAGE DRAWING (UNIT: mm)



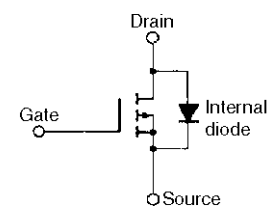
Electrode connection

- <1> Gate (G)
- <2> Drain (D)
- <3> Source (S)
- <4> Fin (drain)

#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Ratings	Unit
Drain to source voltage	$V_{DS}$	$V_{GS} = 0$	-60	V
Gate to source voltage	$V_{GS}$	$V_{DS} = 0$	$\mp 20$	V
Drain current (DC)	$I_{D(DC)}$	$T_c = 25^\circ\text{C}$	$\mp 2.0$	A
Drain current (pulse)	$I_{D(pulse)}$	$PW \leq 300\ \mu\text{s}$ duty cycle $\leq 10\%$	$\mp 8.0$	A
Total power dissipation	$P_T$	$T_c = 25^\circ\text{C}$	20	W
Total power dissipation	$P_T$	$T_a = 25^\circ\text{C}$	1.0*, 2.0**	W
Channel temperature	$T_{ch}$		150	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

#### INTERNAL EQUIVALENT CIRCUIT



\* Printing board mounted

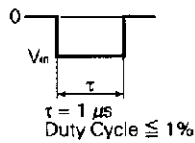
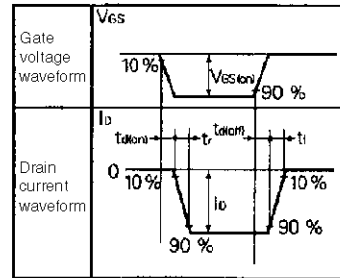
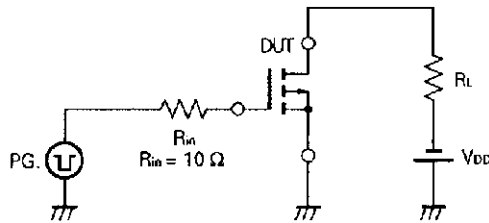
\*\*  $7.5\text{ cm}^2 \times 0.7\text{ mm}$  ceramic board mounted

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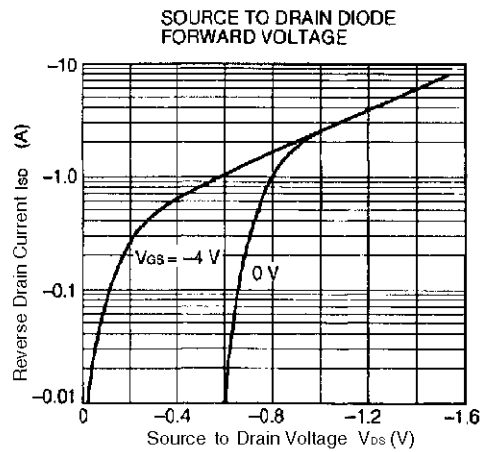
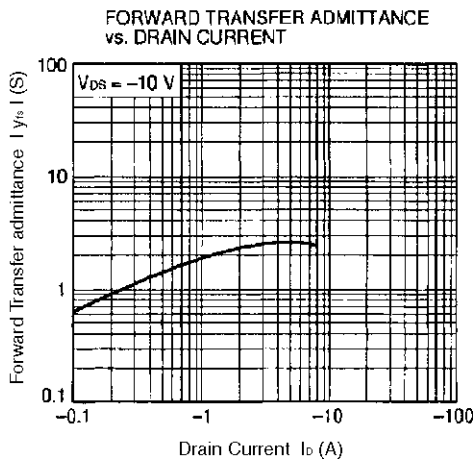
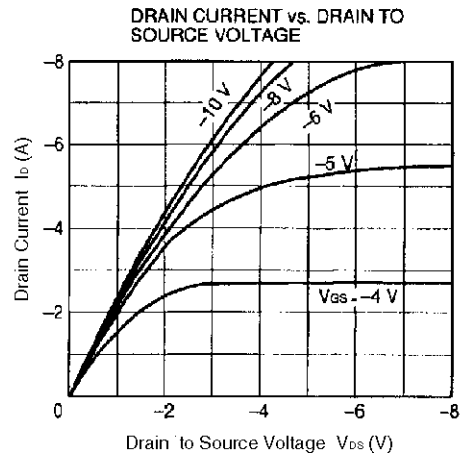
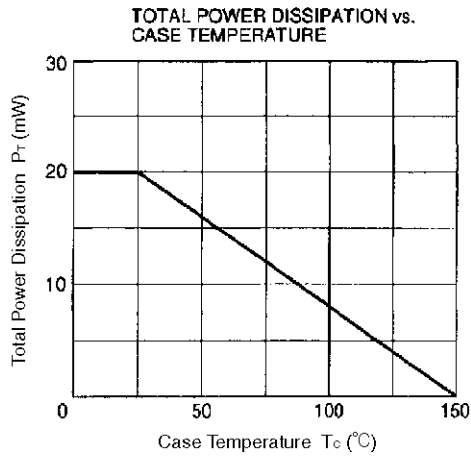
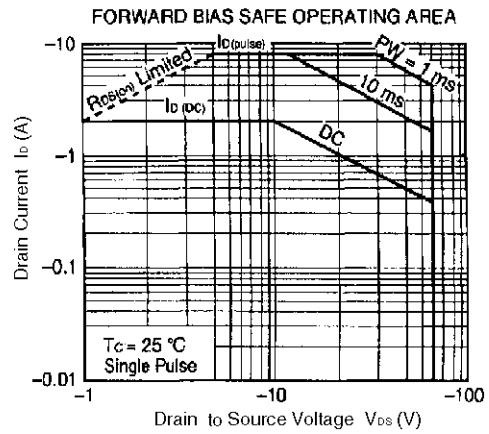
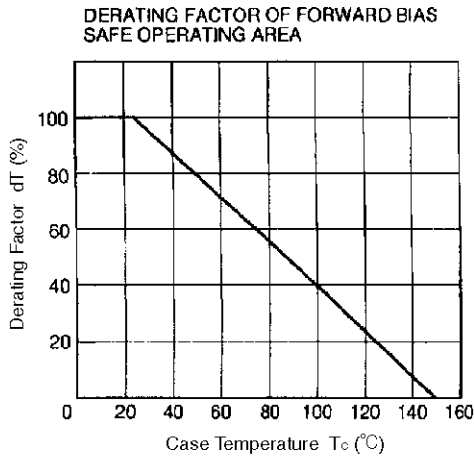
**ELECTRICAL CHARACTERISTICS (Ta = 25°C)**

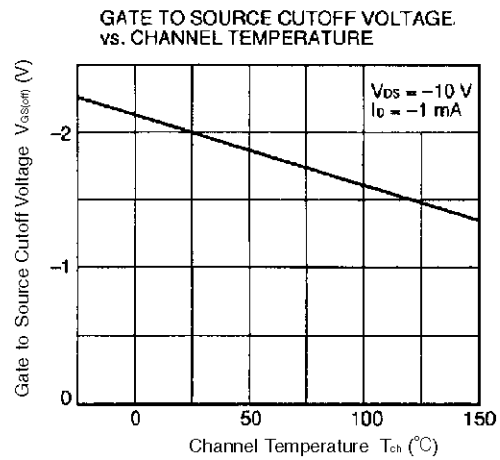
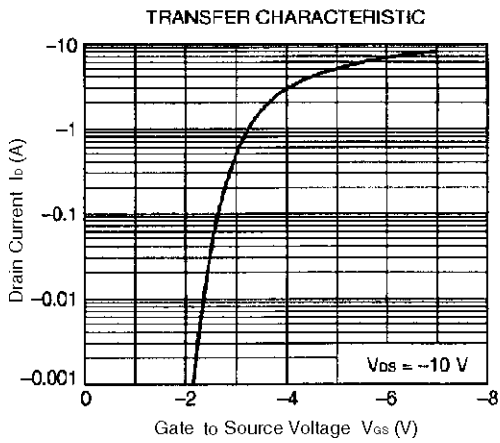
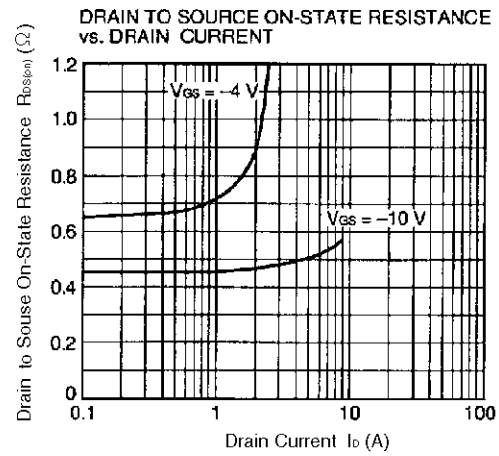
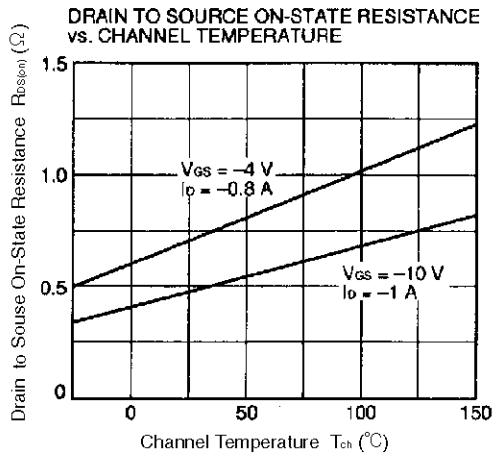
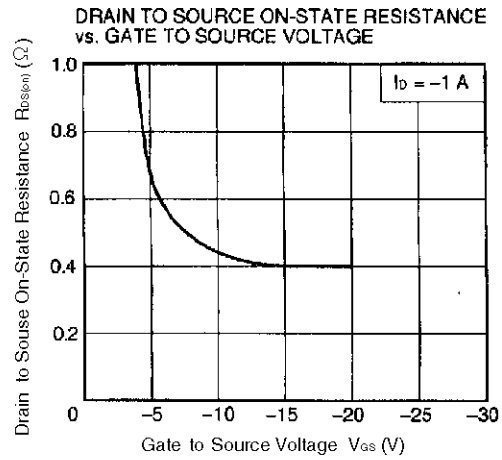
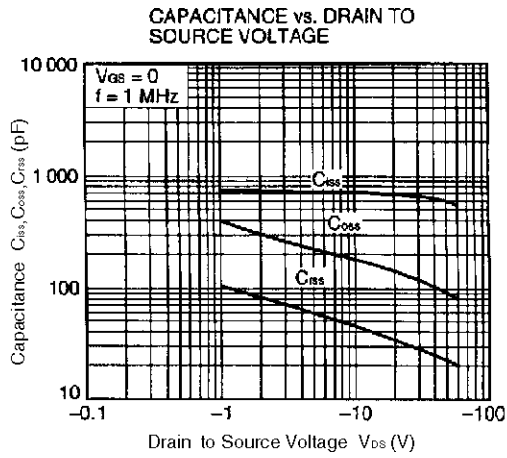
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Drain cutoff current	$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0$			-10	$\mu\text{A}$
Gate cutoff current	$I_{GSS}$	$V_{GS} = \mp 20\text{ V}, V_{DS} = 0$			$\mp 100$	nA
Gate cutoff voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1.0\text{ mA}$	-1.0	-2.0	-3.0	V
Forward transfer admittance	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -1.0\text{ A}$	1.0	1.8		S
Drain to source on-state resistance	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -1.0\text{ A}$		0.45	0.8	$\Omega$
Drain to source on-state resistance	$R_{DS(on)2}$	$V_{GS} = -4\text{ V}, I_D = -0.8\text{ A}$		0.7	1.3	$\Omega$
Input capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$		660		pF
Output capacitance	$C_{oss}$			250		pF
Reverse transfer capacitance	$C_{rss}$			50		pF
Turn-on delay time	$t_{d(on)}$	$I_D = -1.0\text{ A}, V_{GS(on)} = -10\text{ V}$ $V_{DD} \cong -30\text{ V}, R_L = 30\ \Omega,$ $R_{in} = 10\ \Omega$		30		ns
Rise time	$t_r$			30		ns
Turn-off delay time	$t_{d(off)}$			110		ns
Fall time	$t_f$			40		ns

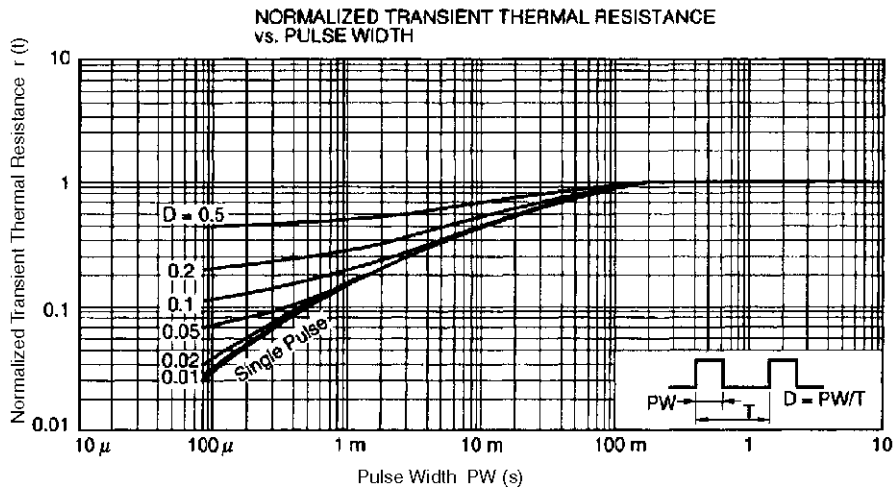
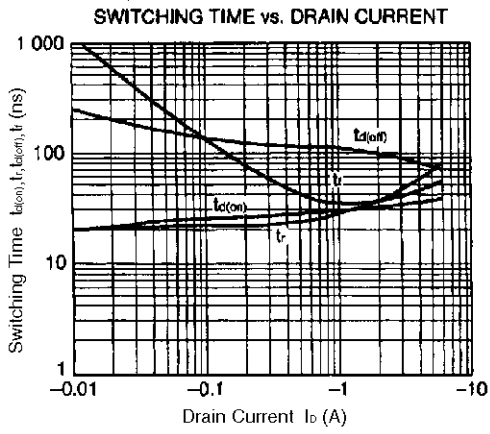
**SWITCHING TIME TEST CIRCUIT, TEST CONDITION (RESISTANCE LOAD)**



TYPICAL CHARACTERISTICS (Ta = 25°C)







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