
2SJ317

Silicon P-Channel MOS FET

HITACHI

Application

High speed power switching

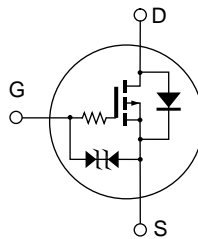
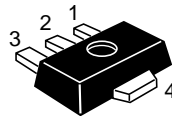
Low voltage operation

Features

- Very low on-resistance
- High speed switching
- Suitable for camera or VTR motor drive circuit, power switch, solenoid drive and etc.

Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

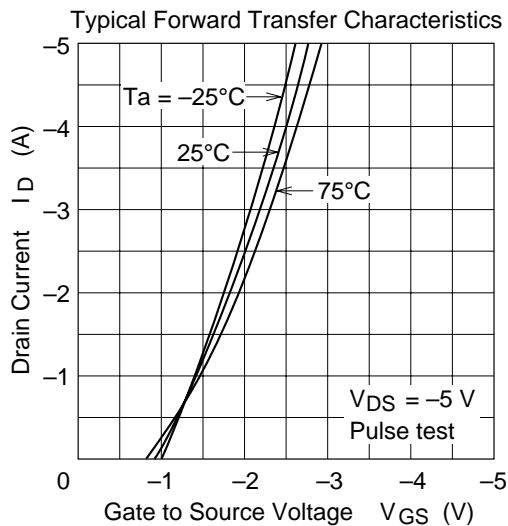
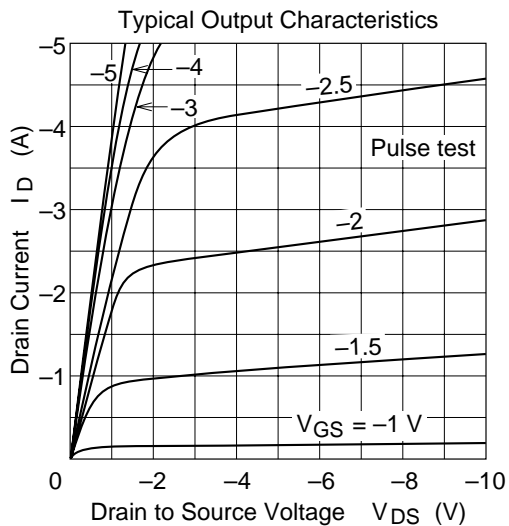
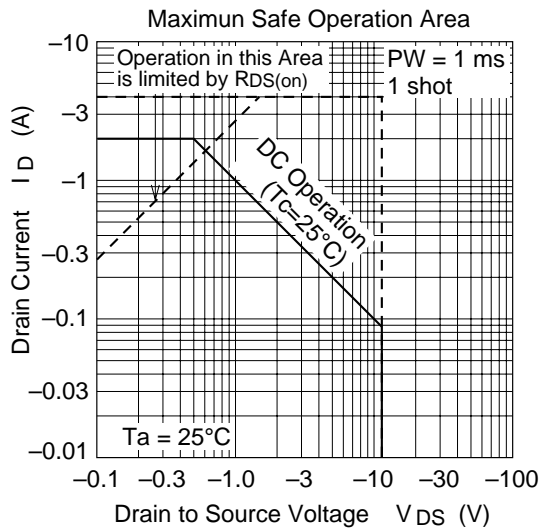
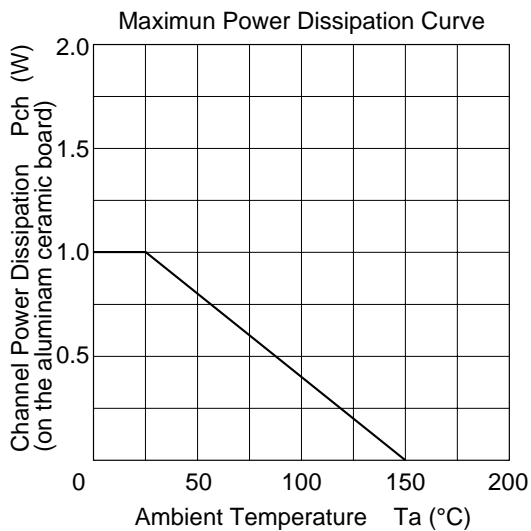
Item	Symbol	Rated	Unit
Drain to source voltage	V_{DSS}	-12	V
Gate to source voltage	V_{GSS}	-7	V
Drain current	I_D	±2	A
Drain peak current	$I_{D(pulse)}^{*1}$	±4	A
Body to drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch^{*2}	1	W
Channel temperature	Tch	150	°C
Storage temperature	$Tstg$	-55 to +150	°C

- Notes: 1. $PW \leq 100 \mu s$, duty cycle $\leq 10\%$
 2. Value on the alumina ceramic board (12.5×20×0.7 mm).
 3. Marking is "NY".

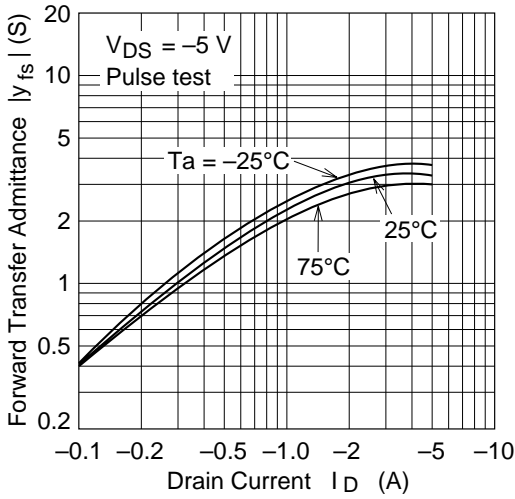
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-12	—	—	V	$I_D = -1 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±7	—	—	V	$I_G = \pm 10 \mu A$, $V_{DS} = 0$
Gate to source cutoff current	I_{GSS}	—	—	±5	μA	$V_{GS} = \pm 6.5 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -8 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$I_D = -100 \mu A$, $V_{DS} = -5 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)1}$	—	0.4	0.7	Ω	$I_D = -0.5 \text{ A}^{*1}$, $V_{GS} = -2.2 \text{ V}$
	$R_{DS(on)2}$	—	0.28	0.35	Ω	$I_D = -1 \text{ A}^{*1}$, $V_{GS} = -4 \text{ V}$
Forward transfer admittance	$ y_{fs} $	1.0	2.3	—	S	$I_D = -1 \text{ A}^{*1}$, $V_{DS} = -5 \text{ V}$
Input capacitance	C_{iss}	—	63	—	pF	$V_{DS} = -5 \text{ V}$, $V_{GS} = 0$,
Output capacitance	C_{oss}	—	180	—	pF	$f = 1 \text{ MHz}$
Reverse transfer capacitance	C_{rss}	—	23	—	pF	
Turn-on time	t_{on}	—	500	—	ns	$I_D = -0.2 \text{ A}^{*1}$, $V_{in} = -4 \text{ V}$,
Turn-off time	t_{off}	—	2860	—	ns	$R_L = 51 \Omega$

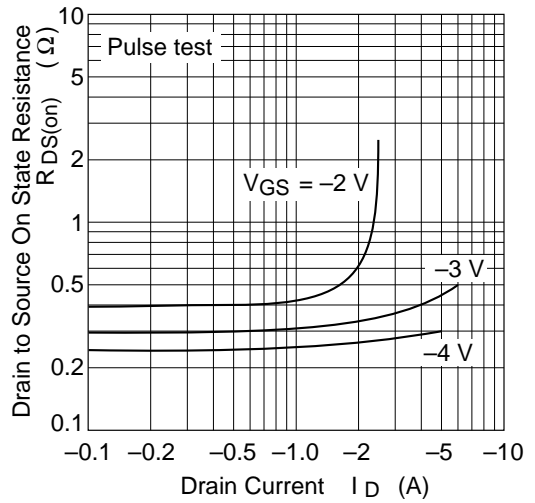
- Note: 1. Pulse test



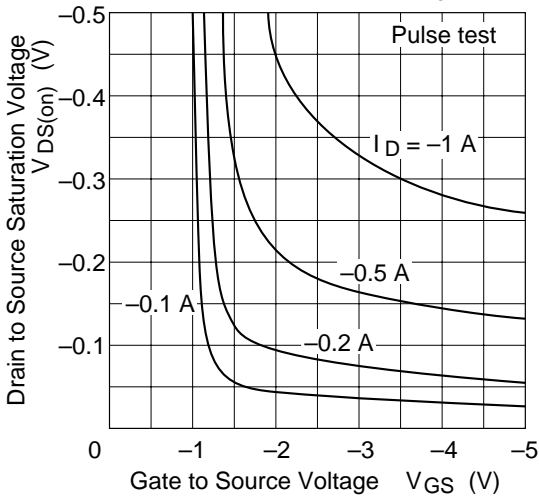
Forward Transfer Admittance vs. Drain Current



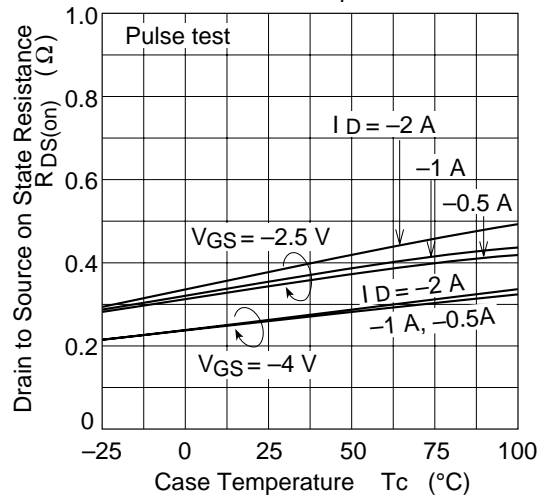
Drain to Source on State Resistance vs. Drain Current



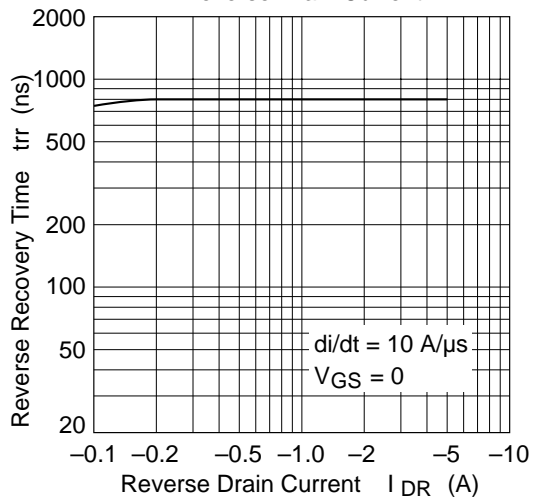
Drain to Source Saturation Voltage vs. Gate to Source Voltage



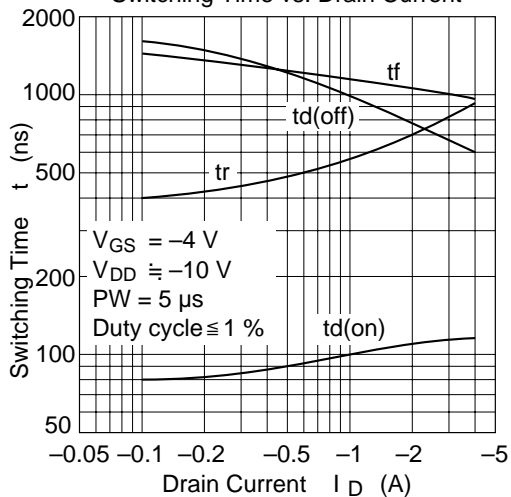
Drain to Source on State Resistance vs. Case Temperature



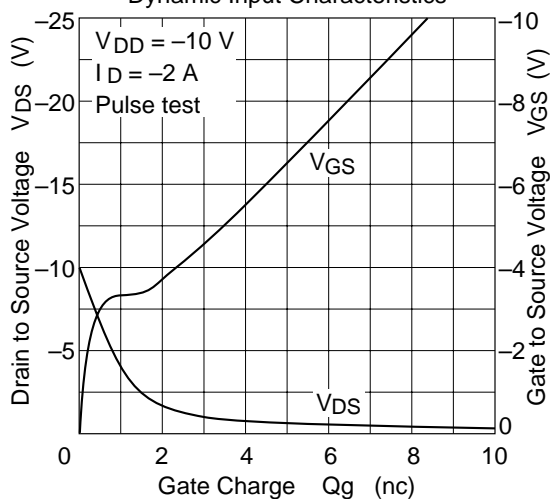
Reverse Recovery Time vs.
Reverse Drain Current



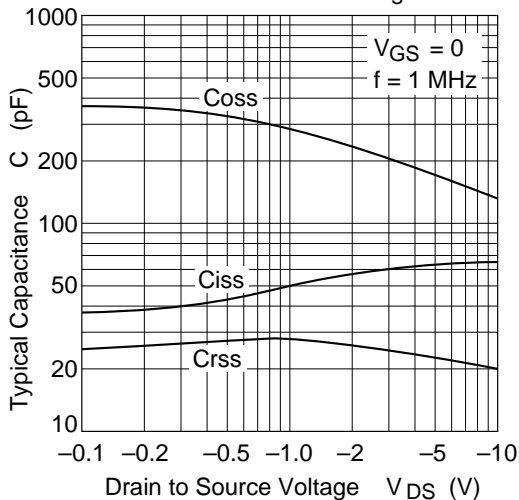
Switching Time vs. Drain Current

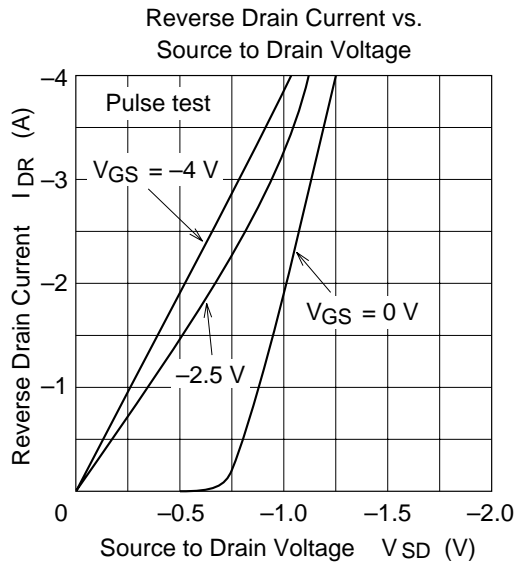


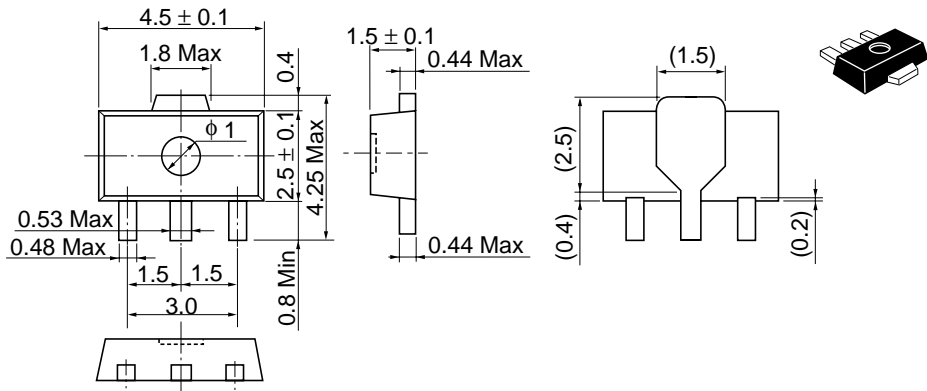
Dynamic Input Characteristics



Typical Capacitance vs.
Drain to Source Voltage







Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.050 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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