

MOS FIELD EFFECT TRANSISTOR



SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ324 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

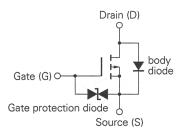
- · Low On-state Resistance
 - $R_{DS(on)} = 0.18 \Omega \text{ TYP}. \text{ (VGS} = -10 \text{ V, ID} = -1.0 \text{ A)}$ $R_{DS(on)} = 0.36 \Omega \text{ TYP.}$ (Vgs = -4 V, ID = -0.8 A)
- Low Ciss: Ciss = 330 pF TYP.
- · Built-in G-S Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

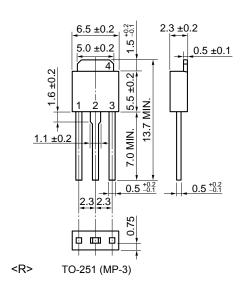
Drain to Source Voltage	VDSS	-30	V
Gate to Source Voltage (AC)	V _{GSS}	∓20	V
Gate to Source Voltage (DC)	V _{GSS}	-20, +10	V
Drain Current (DC)	I _{D(DC)}	∓2.0	Α
Drain Current (pulse) Note	I _{D(pulse)}	∓8.0	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	20	W
Total Power Dissipation (T _A = 25°C)	P_{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

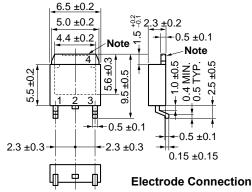
Note PW \leq 10 μ s, Duty Cycle \leq 1%

EQUIVALENT CIRCUIT



PACKAGE DRAWINGS (Unit: mm)





- 1. Gate
- 2. Drain
- TO-252 (MP-3Z)
- 3. Source
- 4. Drain Fin

Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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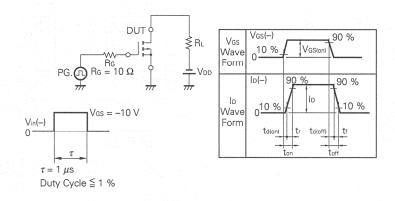
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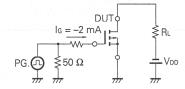
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-state Resistance	RDS(on)		0.18	0.25	Ω	Vgs = -10 V, ID = -1.0 A	
Drain to Source On-state Resistance	Ros(on)		0.36	0.52	Ω	Vgs = -4 V, ID = -0.8 A	
Gate to Source Cutoff Voltage	VGS(off)	-1.0	-1.5	-2.0	V	V _{DS} = −10 V, I _D = −1 mA	
Forward Transfer Admittance	y fs	1.0	1.9		S	V _{DS} = -10 V, I _D = -1.0 A	
Drain Leakage Current	Inss			-10	μΑ	Vps = -30 V, Vgs = 0	
Gate to Source Leakage Current	Igss			±10	μΑ	Vgs = ∓16 V, Vps = 0	
Input Capacitance	Ciss		330		рF	Vps = -10 V	
Output Capacitance	Coss		290		pF	V _{GS} = 0 f = 1 MHz	
Reverse Transfer Capacitance	Crss		105		рF		
Turn-On Delay Time	td(on)		. 7		ns	$V_{GS(on)} = -10 \text{ V}$ $V_{DD} = -15 \text{ V}$	
Rise Time	tr		35		ns		
Turn-Off Delay Time	td(off)		40		ns	$ID = -1.0 \text{ A, Rg} = 10 \Omega$ $RL = 15 \Omega$	
Fall Time	tf		30	g/1 / .	ns		
Total Gate Charge	Qg		12		nC	Vcs = -10 V Ib = -2.0 A Vbb = -24 V	
Gate to Source Charge	Qgs		1.5		nC		
Gate to Drain Charge	QgD		4.5		nC		
Body Diode Forward Voltage	VF		0.9		V	IF = 2.0 A, VGS = 0	
Reverse Recovery Time	trr		50		ns	Ir = 2.0 A, Vas = 0 di/dt = 50 A/μs	
Reverse Recovery Charge	Qrr		40		nC		
ESD	VESD		±130	1	V	C = 200 pF, R = 0, Single Puls	

Test Circuit 1: Switching Time



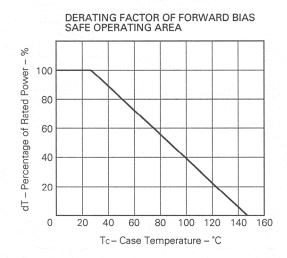
Test Circuit 2: Gate Charge





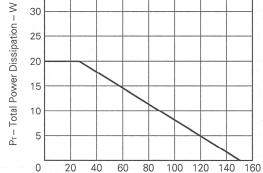


TYPICAL CHARACTERISTICS (Ta = 25 °C)



CASE TEMPERATURE 35 30

TOTAL POWER DISSIPATION vs.



0

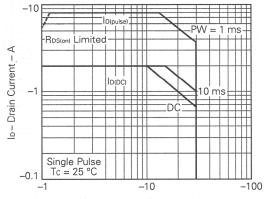
 10μ

Tc - Case Temperature - °C

 100μ

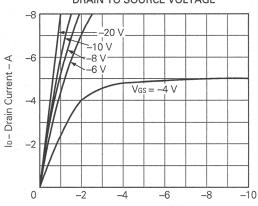
1 m

FORWARD BIAS SAFE OPERATING AREA



V_{DS} - Drain to Source Voltage - V

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



V_{DS} - Drain to Source Voltage - V

10

100

rtn(t) - Transient Thermal Resistance - °C/W 1000 Channel to Ambient Rth(ch-a) = 125 (°C/W) 100 10 Channel to Case Rth(ch-c) = 6.25 (°C/W) Single Pulse

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

PW -Pulse Width - s

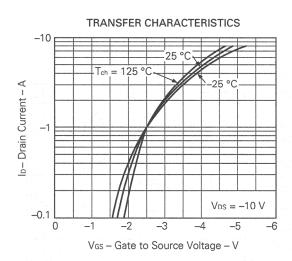
100 m

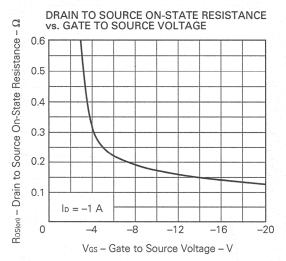
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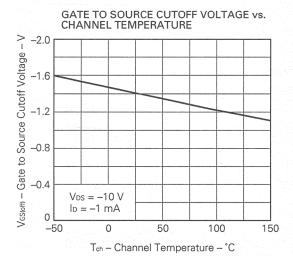
10 m



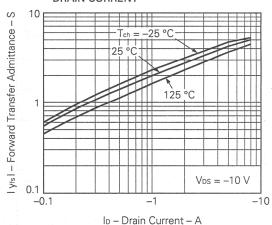
Phase-out/Discontinued



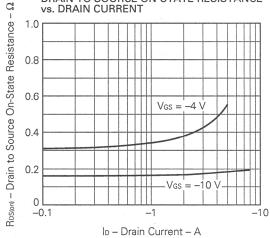




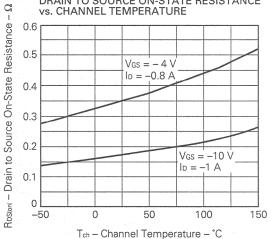




DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

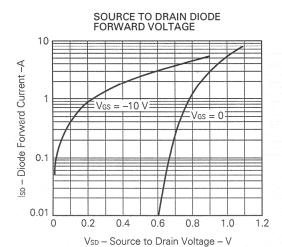


Data Sheet D18327EJ3V0DS

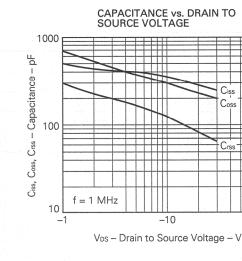


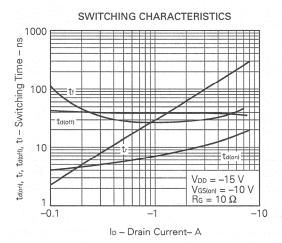
-100

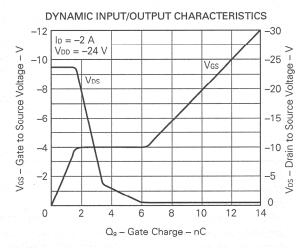


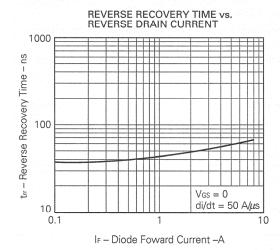


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NEC 2SJ324,324-Z

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