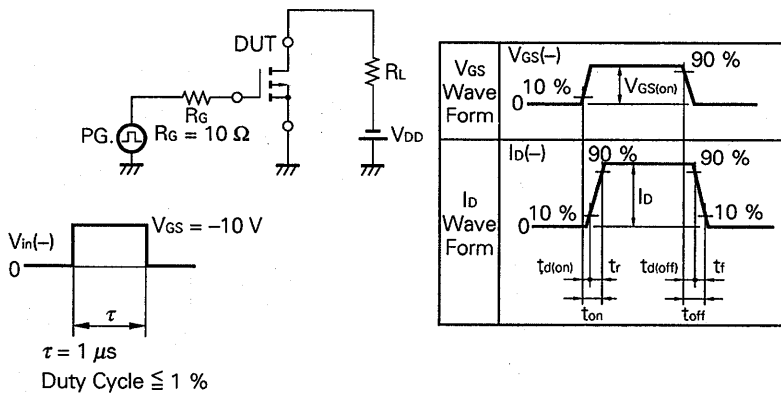


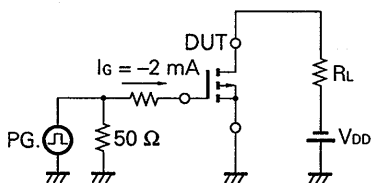
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.28	0.37	Ω	V _{GS} = -10 V, I _D = -1.0 A
Drain to Source On-state Resistance	R _{DS(on)}		0.50	0.68	Ω	V _{GS} = -4 V, I _D = -0.8 A
Gate to Source Cutoff Voltage	V _{GS(off)}	-1.0	-1.5	-2.0	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs}	1.0	1.8		S	V _{DS} = -10 V, I _D = -1.0 A
Drain Leakage Current	I _{DSS}			-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Input Capacitance	C _{iss}		320		pF	V _{DS} = -10 V
Output Capacitance	C _{oss}		220		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		75		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		5		ns	V _{GS(on)} = -10 V V _{DD} = -30 V I _D = -1.0 A, R _G = 10 Ω R _L = 30 Ω
Rise Time	t _r		15		ns	
Turn-Off Delay Time	t _{d(off)}		40		ns	
Fall Time	t _f		25		ns	
Total Gate Charge	Q _G		12		nC	V _{GS} = -10 V I _D = -2.0 A V _{DD} = -48 V
Gate to Source Charge	Q _{GS}		1		nC	
Gate to Drain Charge	Q _{GD}		5		nC	
Body Diode Forward Voltage	V _F		0.9		V	I _F = 2.0 A, V _{GS} = 0
ESD	V _{ESD}		±130		V	C = 200 pF, R = 0, Single Pulse
Reverse Recovery Time	t _{rr}		72		ns	I _F = 2.0 A, V _{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		30		nC	

Test Circuit 1: Switching Time

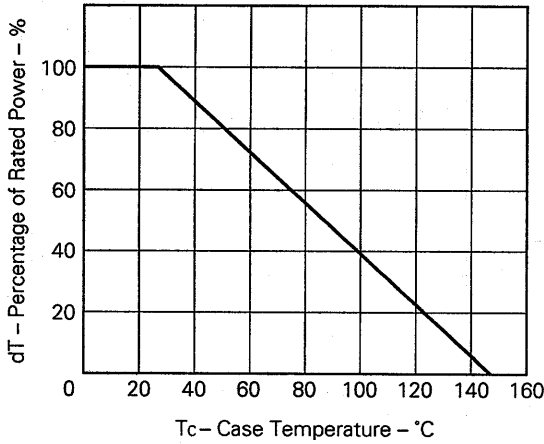


Test Circuit 2: Gate Charge

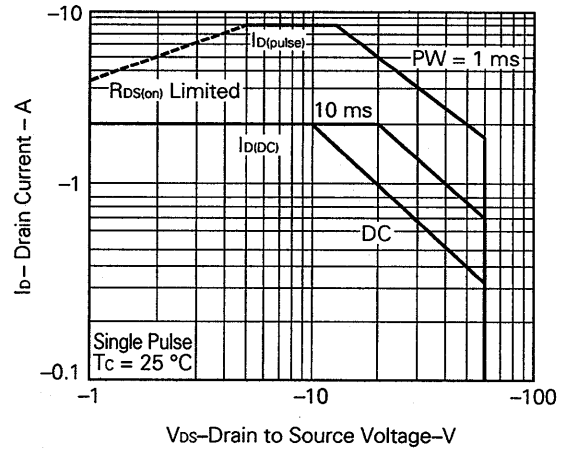


ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$)

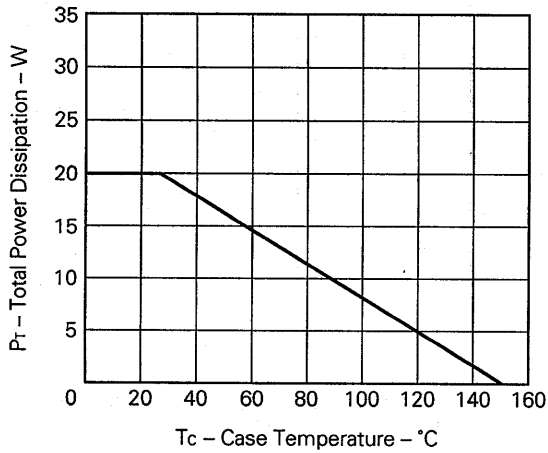
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



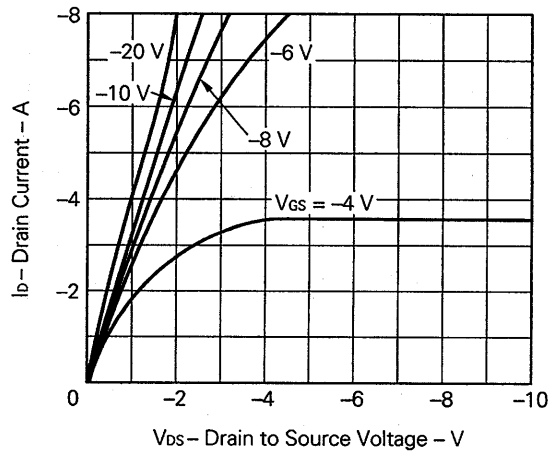
FORWARD BIAS SAFE OPERATING AREA



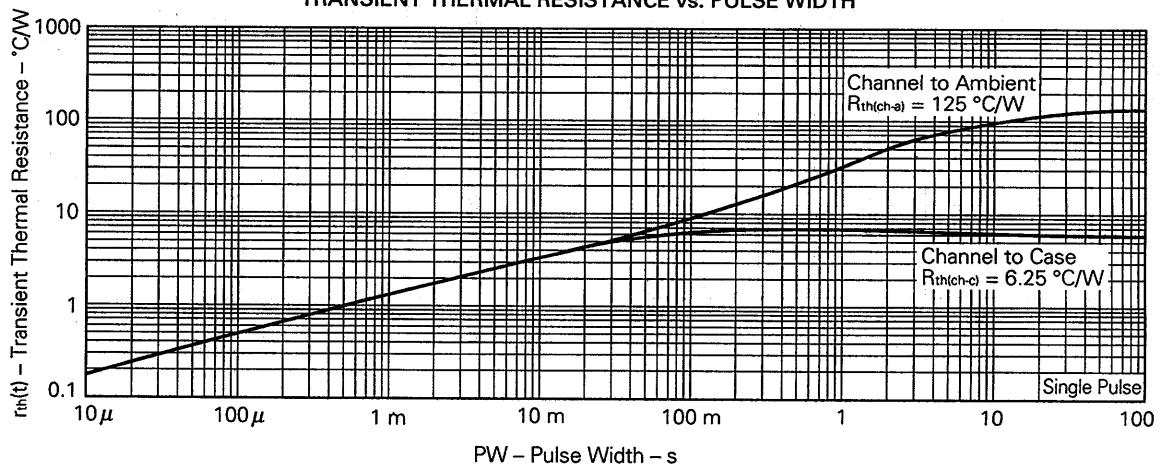
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



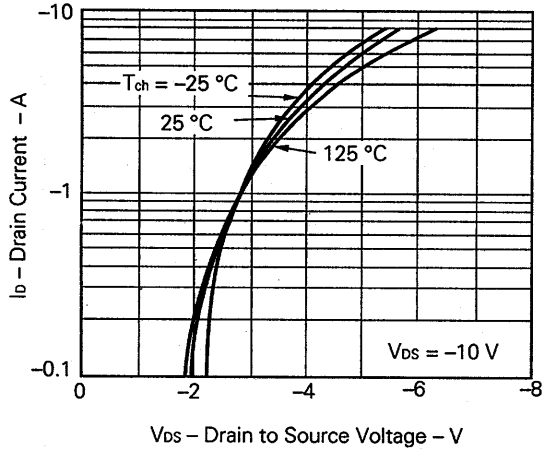
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



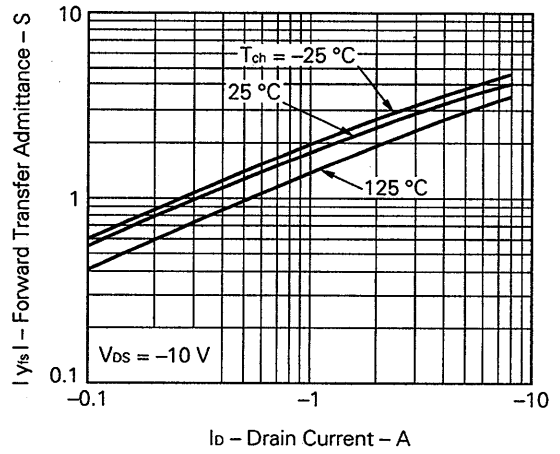
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



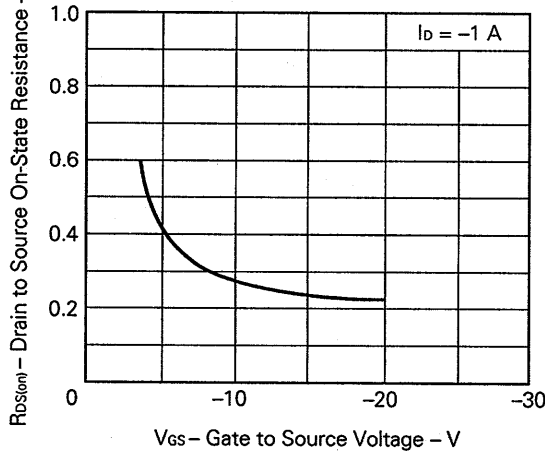
TRANSFER CHARACTERISTICS



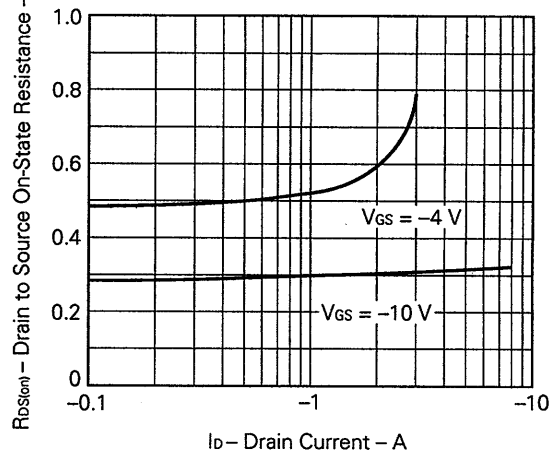
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



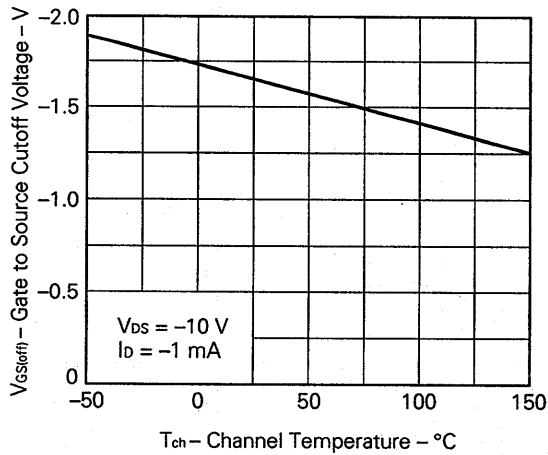
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



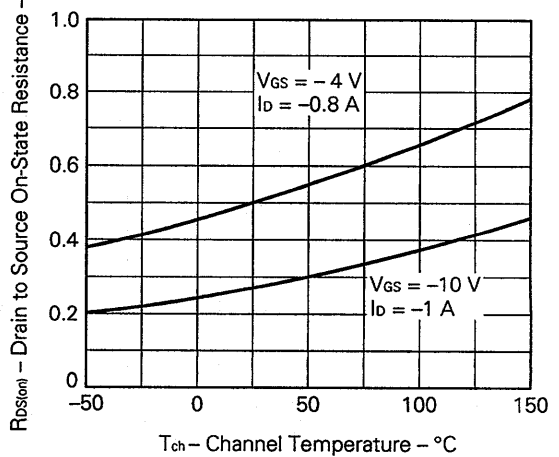
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



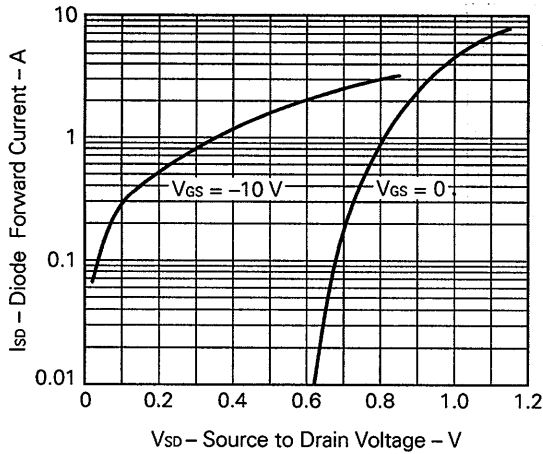
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



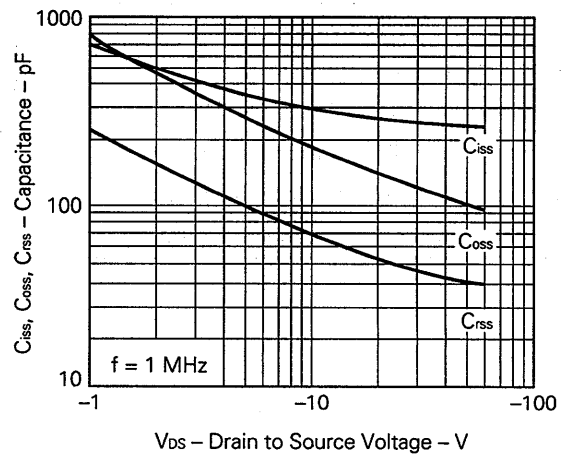
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



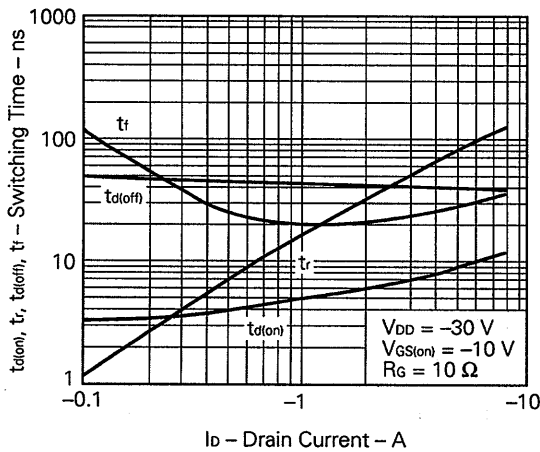
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



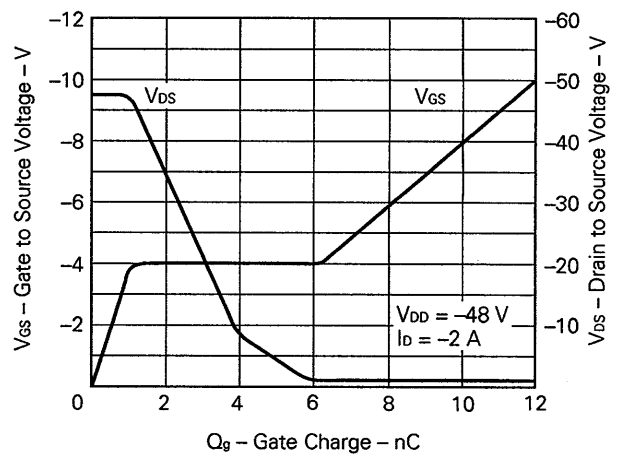
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



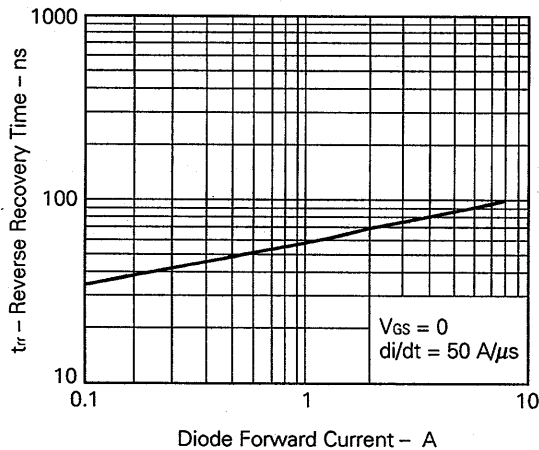
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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