
2SJ450

Silicon P-Channel MOS FET

HITACHI

ADE-208-381
1st. Edition

Application

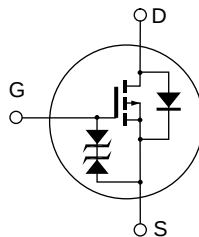
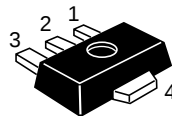
High speed power switching

Features

- Low on-resistance.
- Low drive power
- High speed switching
- 2.5 V gate drive device.

Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	−60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	−1	A
Drain peak current	I _{D(pulse)} ^{*1}	−2	A
Drain peak current	I _{DR}	−1	A
Channel dissipation	Pch ^{*2}	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

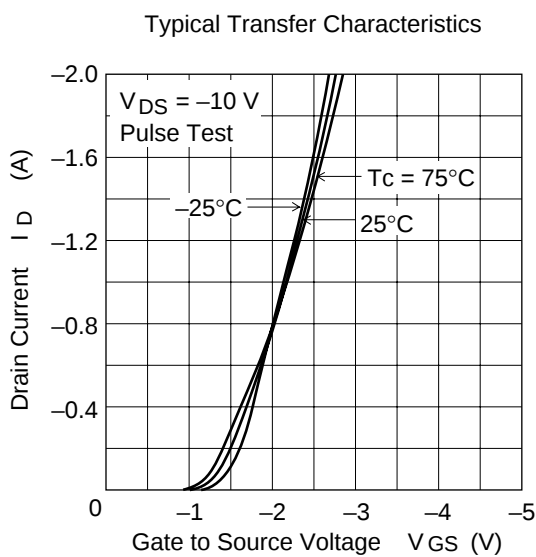
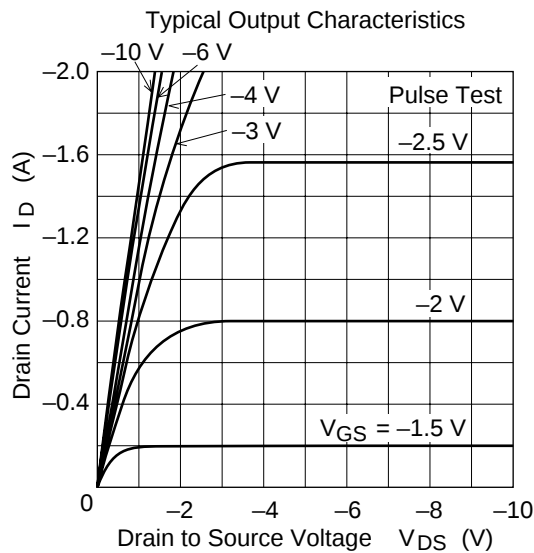
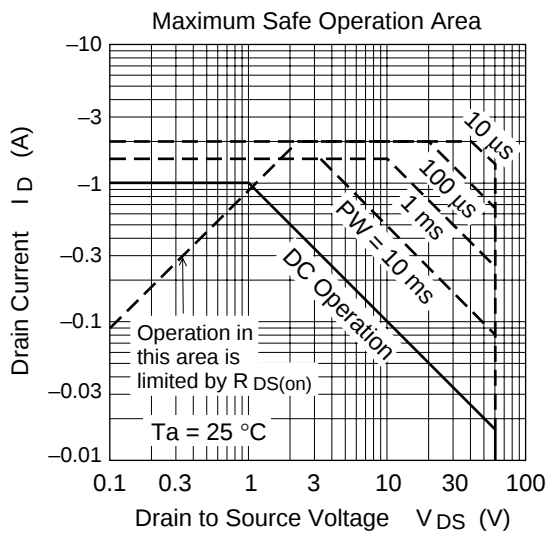
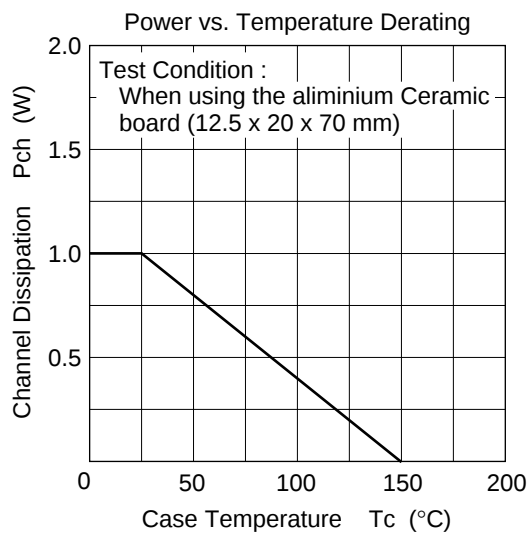
Notes: 1. PW ≤ 100 μs, duty cycle ≤ 10%
2. When using aluminium ceramic board (12.5 × 20 × 70 mm)

Electrical Characteristics (Ta = 25°C)

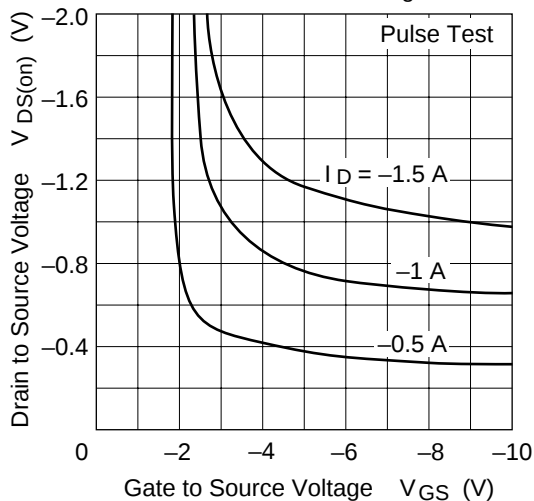
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-50	μA	$V_{DS} = -50 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.5	—	-1.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.85	1.2	Ω	$I_D = -0.5 \text{ A}$ $V_{GS} = -4 \text{ V}^{*1}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.9	Ω	$I_D = -0.3 \text{ A}$ $V_{GS} = -2.5 \text{ V}^{*1}$
Fowerd transfer admittance	$ y_{fs} $	0.6	1.0	—	S	$I_D = -0.5 \text{ A}$ $V_{DS} = -10 \text{ V}$
Input capacitance	C_{iss}	—	150	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	72	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	24	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	6	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -0.5 \text{ A}$
Rise time	t_r	—	9	—	ns	$R_L = 60 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	35	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-0.9	—	V	$I_F = -1 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	100	—	ns	$I_F = -1 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 1. Pulse Test

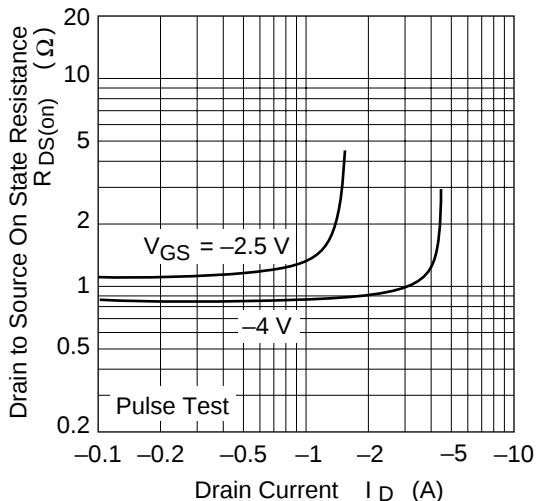
Marking is "UY".



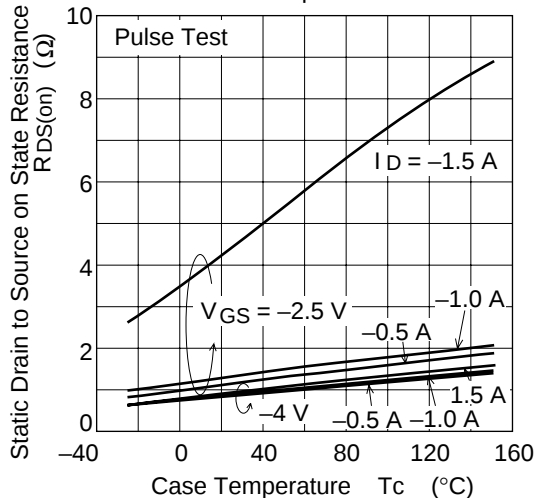
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



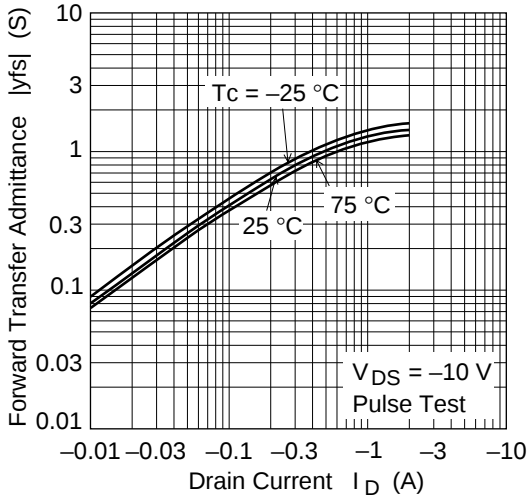
Static Drain to Source on State Resistance
vs. Drain Current



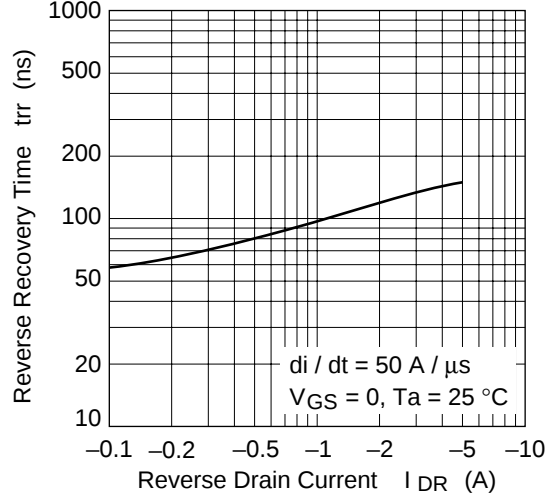
Static Drain to Source on State Resistance
vs. Temperature



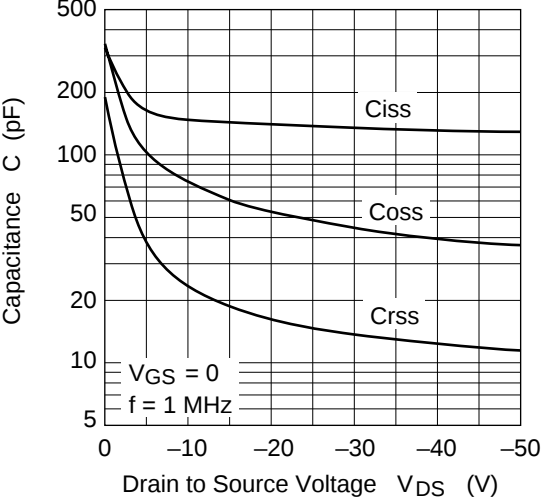
Forward Transfer Admittance vs.
Drain Current



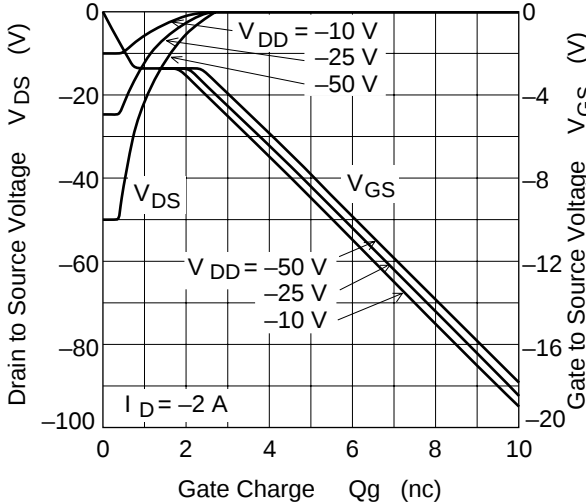
Body to Drain Diode Reverse Recovery Time



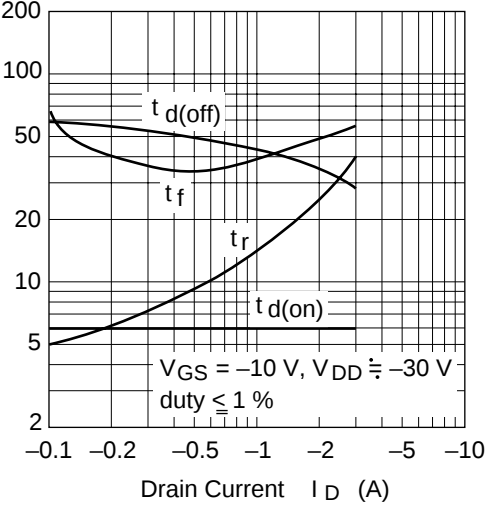
Typical Capacitance vs. Drain to Source Voltage

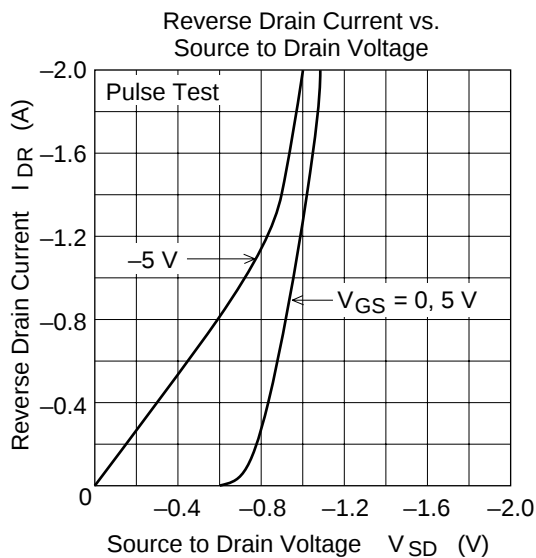


Dynamic Input Characteristics

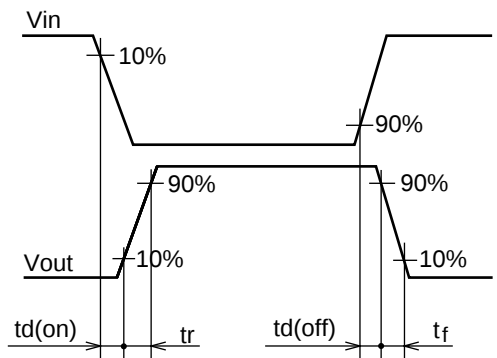
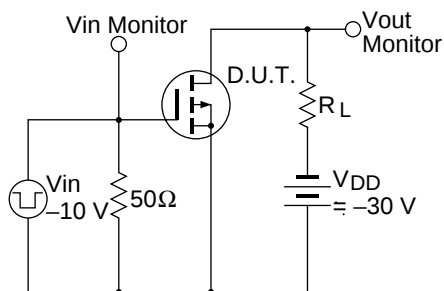


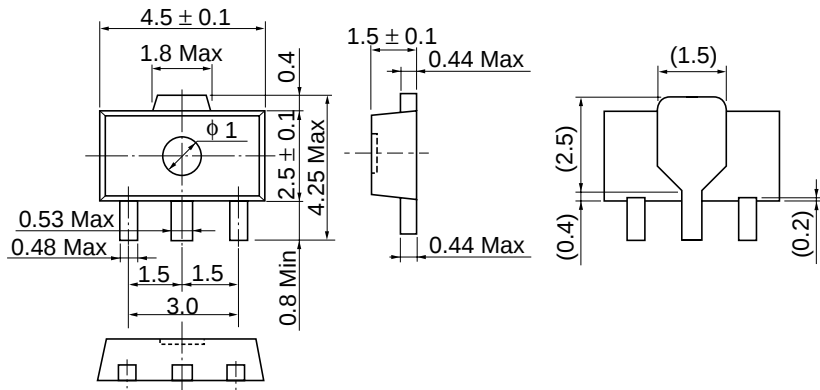
Switching Characteristics





Avalanche Test Circuit and Waveform





Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.050 g

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