

2SJ553(L),2SJ553(S)

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

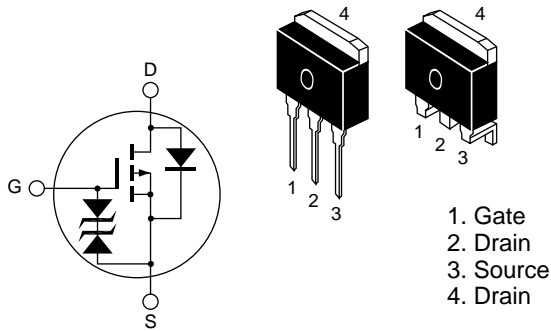
ADE-208-650B (Z)
3rd. Edition
Jun 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.028\Omega$ typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

LDBPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-30	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-120	A
Body-drain diode reverse drain current	I_{DR}	-30	A
Avalanche current	I_{AP} ^{Note3}	-30	A
Avalanche energy	E_{AR} ^{Note3}	77	mJ
Channel dissipation	P_{ch} ^{Note2}	75	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

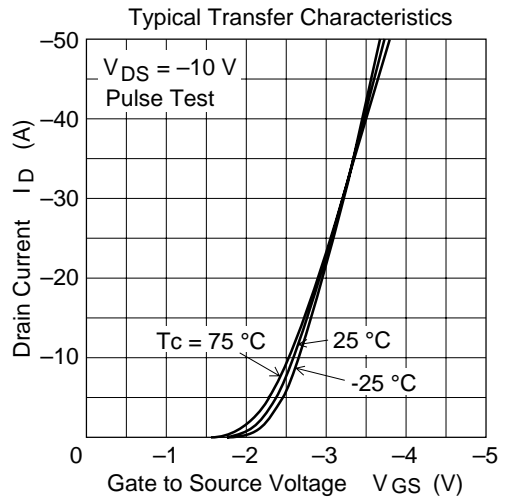
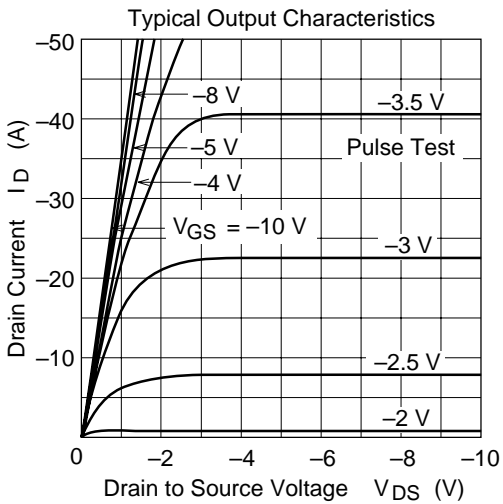
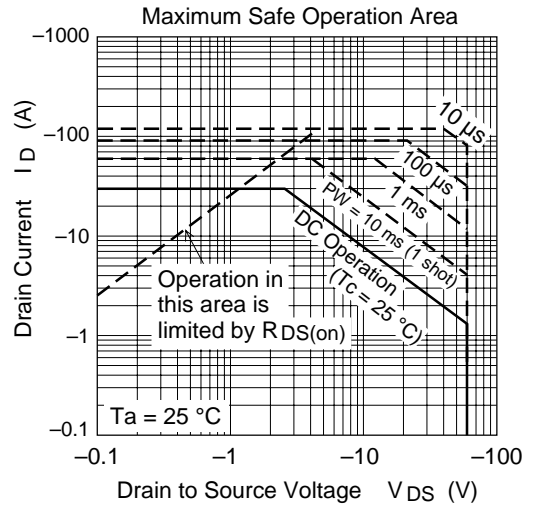
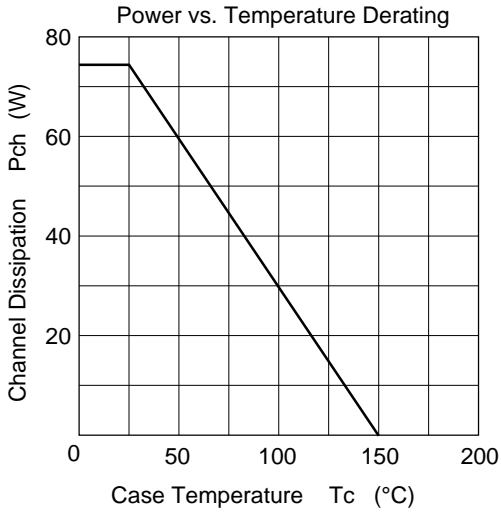
Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

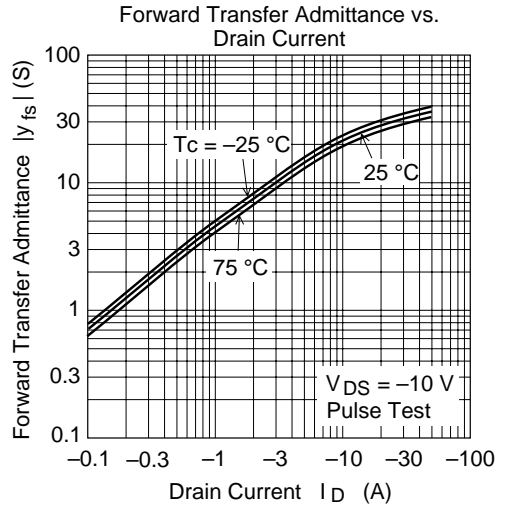
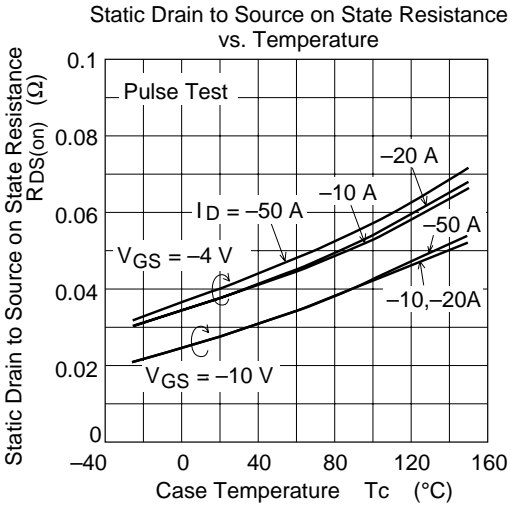
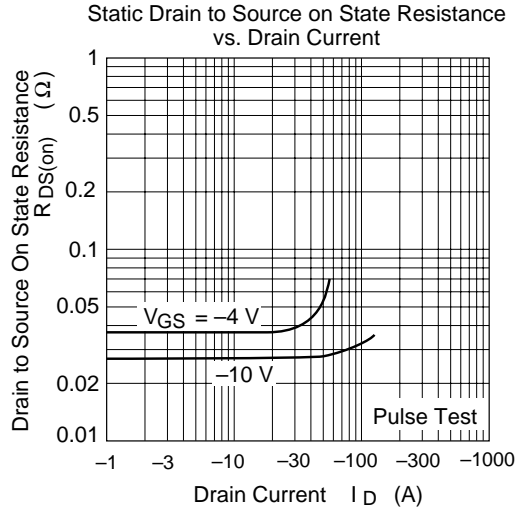
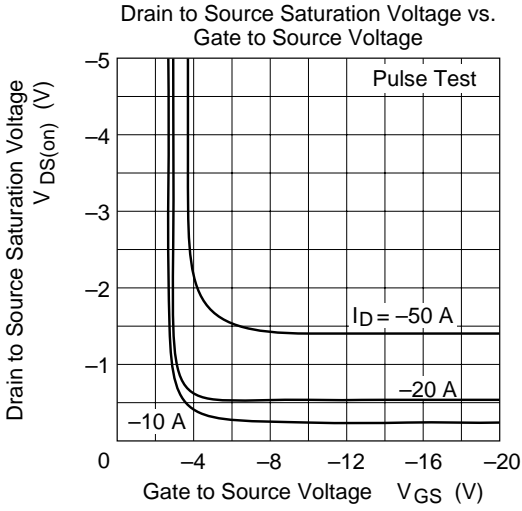
Electrical Characteristics (Ta = 25°C)

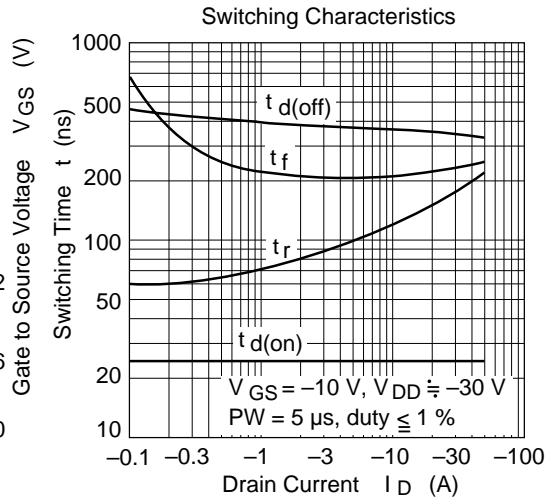
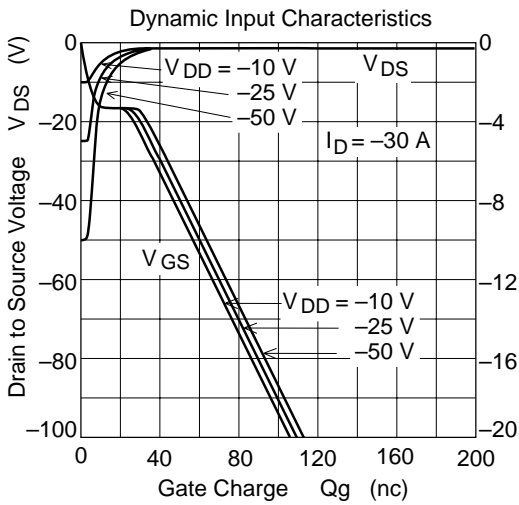
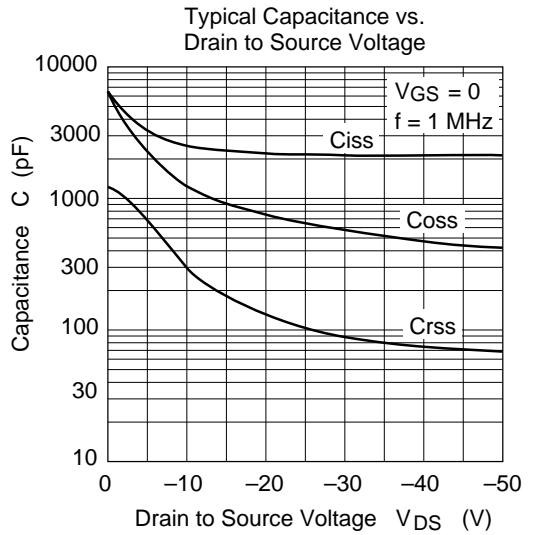
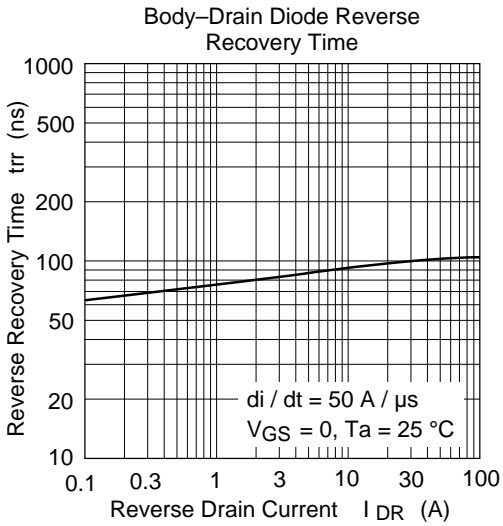
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10mA$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60V$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16V$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1mA$, $V_{DS} = -10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.028	0.037	Ω	$I_D = -15A$, $V_{GS} = -10V$ ^{Note4}
	$R_{DS(on)}$	—	0.038	0.055	Ω	$I_D = -15A$, $V_{GS} = -4V$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	15	25	—	S	$I_D = -15A$, $V_{DS} = -10V$ ^{Note4}
Input capacitance	C_{iss}	—	2500	—	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	—	1300	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	300	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	$V_{GS} = -10V$, $I_D = -15A$
Rise time	t_r	—	150	—	ns	$R_L = 2\Omega$
Turn-off delay time	$t_{d(off)}$	—	350	—	ns	
Fall time	t_f	—	220	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.95	—	V	$I_F = -30A$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	$I_F = -30A$, $V_{GS} = 0$ $di_F/dt = 50A/\mu s$

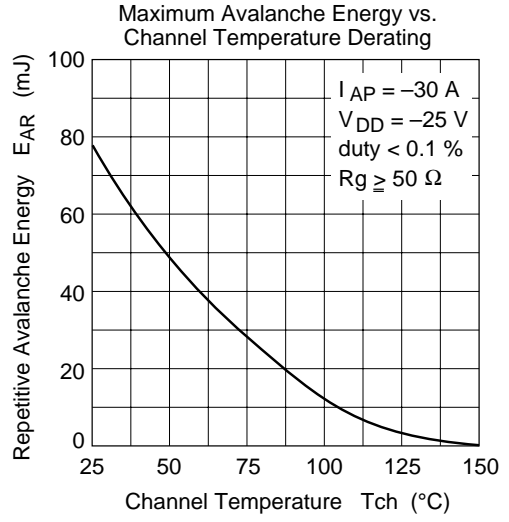
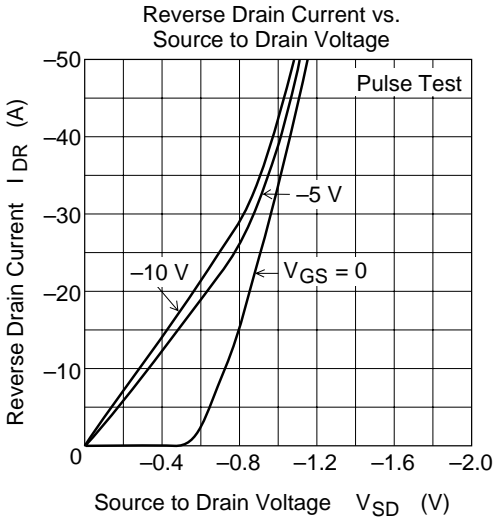
Note: 4. Pulse test

Main Characteristics

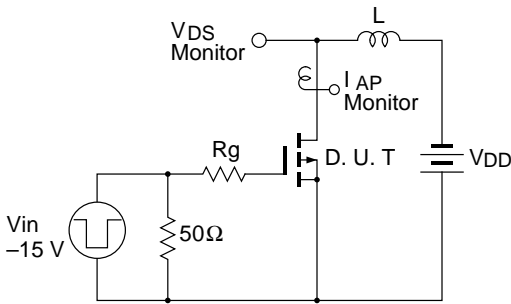






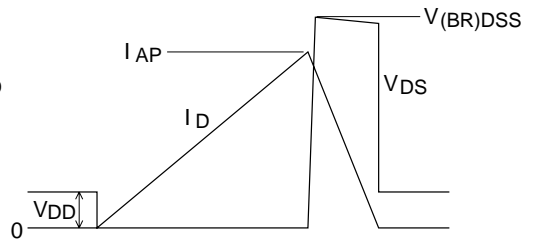


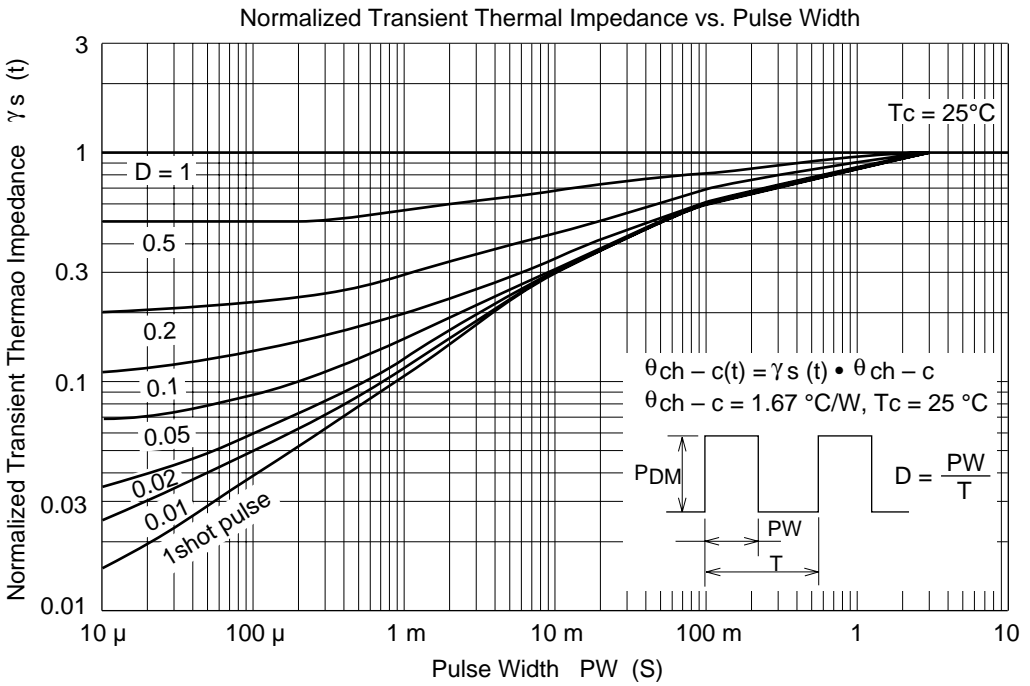
Avalanche Test Circuit



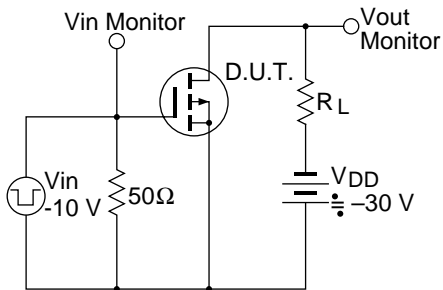
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

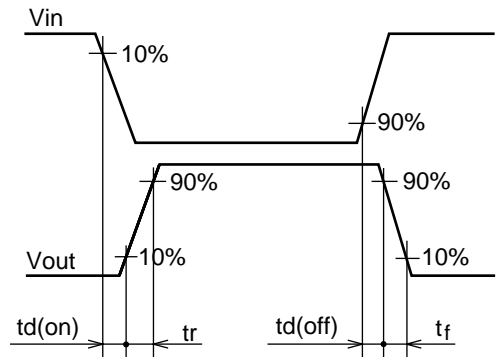




Switching Time Test Circuit

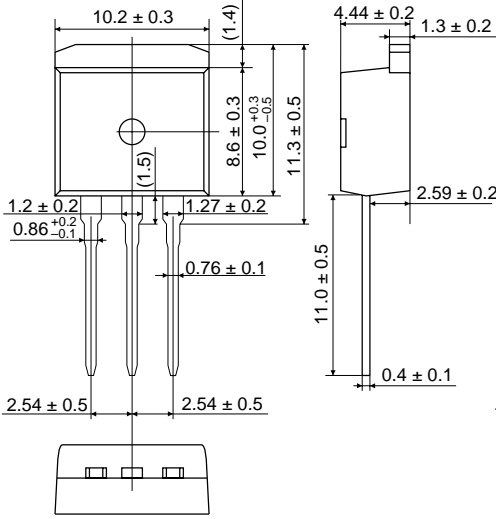


Waveform

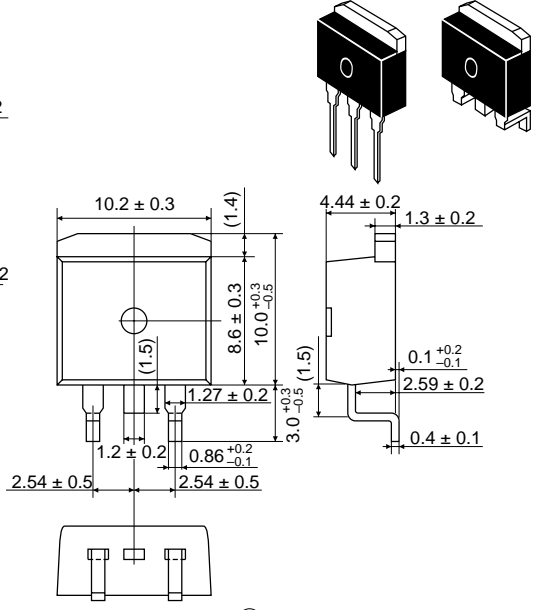


Package Dimensions

Unit: mm



Ⓛ type



Ⓢ type

Hitachi Code	LDBAK
EIAJ	—
JEDEC	—

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