Ordering number:ENN6097A

P-Channel Silicon MOSFET

2SJ563

Ultrahigh-Speed Switching Applications

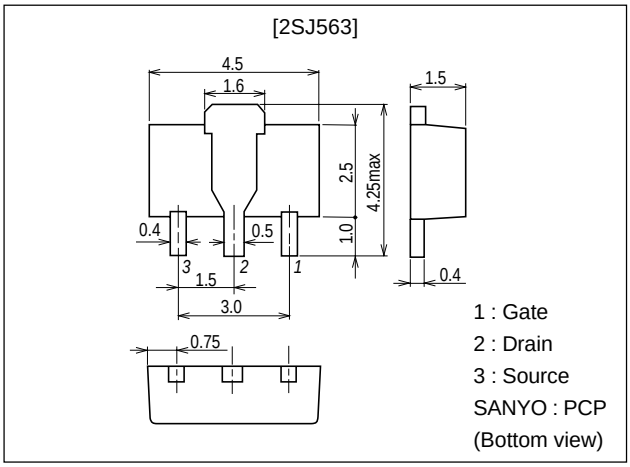
Features

- Low ON-resistance.
- Ultrahigh-speed switching.
- 4V drive.

Package Dimensions

unit:mm

2062A



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		–30	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D		–2	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	–8	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (250mm²×0.8mm)	1.5	W
		Tc=25˚C	3.5	W
Channel Temperature	Tch		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=–1mA, V_{GS}=0	–30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=–30V, V_{GS}=0			–10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=–10V, I_D=–1mA	–1.0		–2.5	V
Forward Transfer Admittance	| yfs |	V_{DS}=–10V, I_D=–1A	1.2	1.7		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)}1$	I_D=–1A, V_{GS}=–10V		240	315	mΩ
	$R_{DS(on)}2$	I_D=–300mA, V_{GS}=–4V		400	550	mΩ

Marking : JO

Continued on next page.

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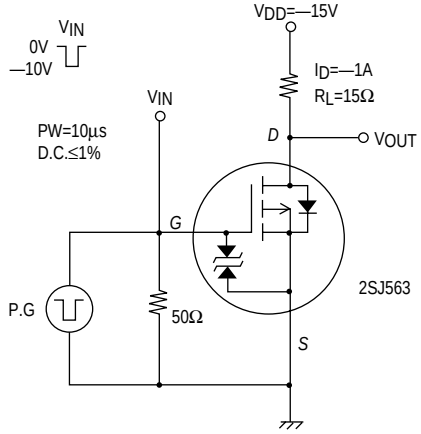
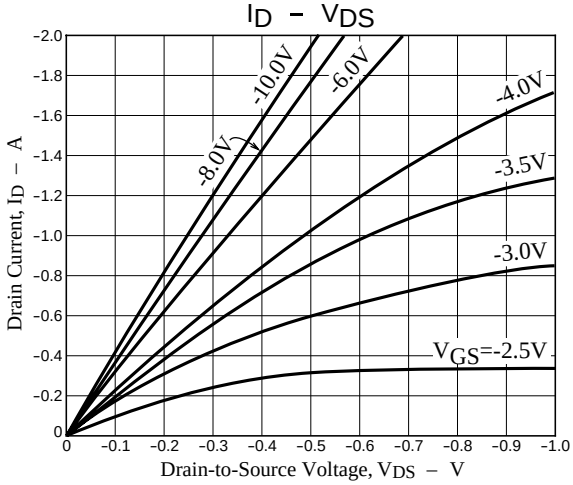
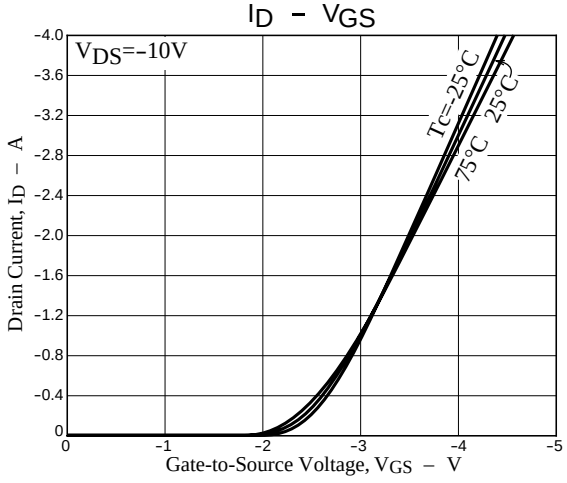
Continued from preceding page.

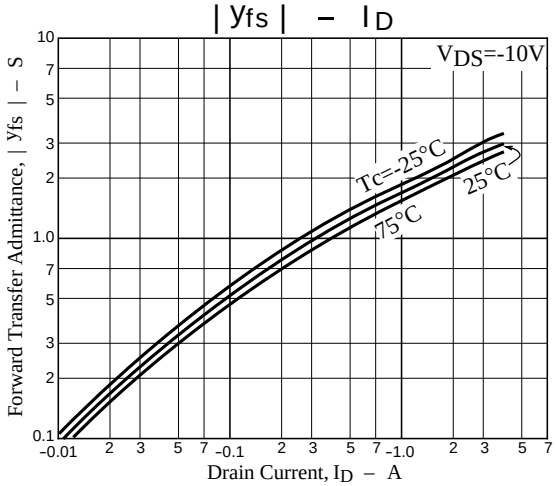
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input Capacitance	Ciss	V_{DS}=–10V, f=1MHz		160		pF
Output Capacitance	Coss	V_{DS}=–10V, f=1MHz		90		pF
Reverse Transfer Capacitance	Crss	V_{DS}=–10V, f=1MHz		38		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit		7		ns
Rise Time	t_r	See specified Test Circuit		7		ns
Turn-OFF Delay Time	$t_{d(off)}$	See specified Test Circuit		23		ns
Fall Time	t_f	See specified Test Circuit		15		ns
Total Gate Charge	Qg	V_{DS}=–10V, V_{GS}=–10V, I_D=–2A		7		nC
Gate-to-Source Charge	Qgs	V_{DS}=–10V, V_{GS}=–10V, I_D=–2A		1		nC
Gate-to-Drain "Miller" Charge	Qgd	V_{DS}=–10V, V_{GS}=–10V, I_D=–2A		1.2		nC
Diode Forward Voltage	V_{SD}	I_S=–2A, V_{GS}=0		–1.0	–1.5	V

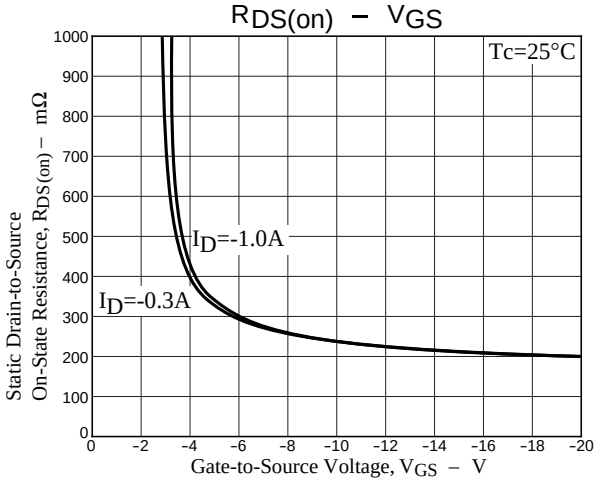
Switching Time Test Circuit



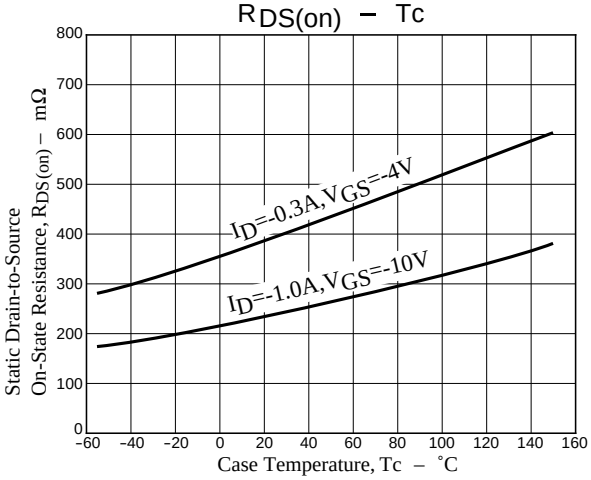




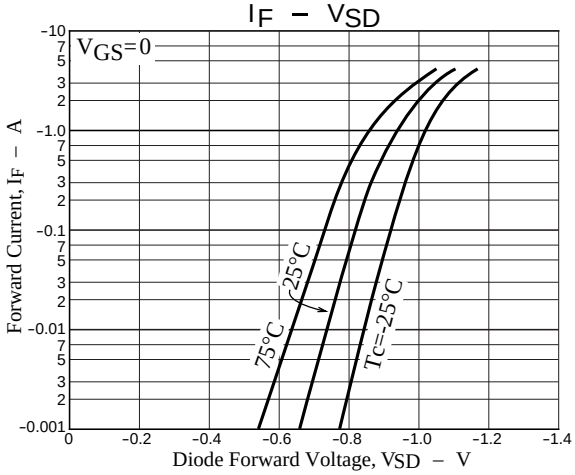




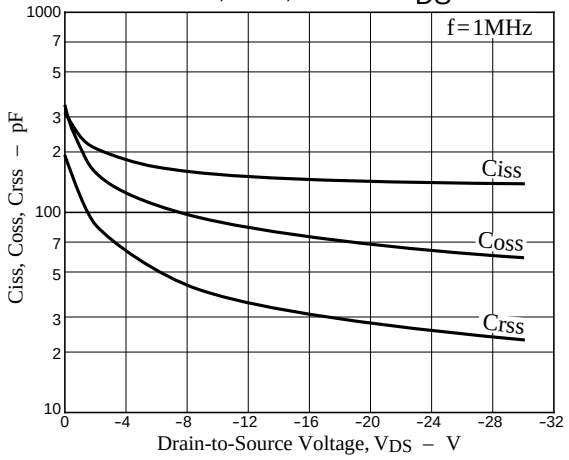
$R_{DS(on)}$ – Tc



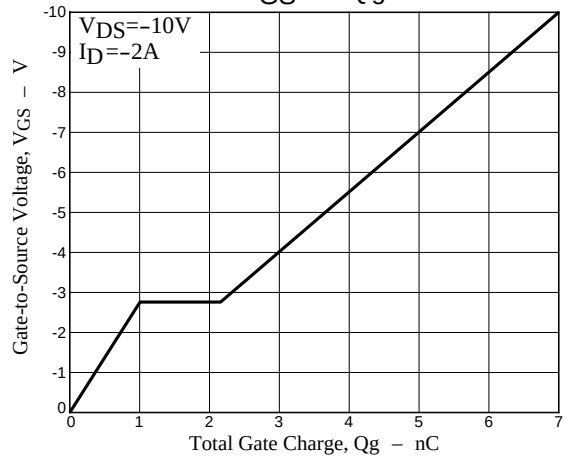
I_F – V_{SD}



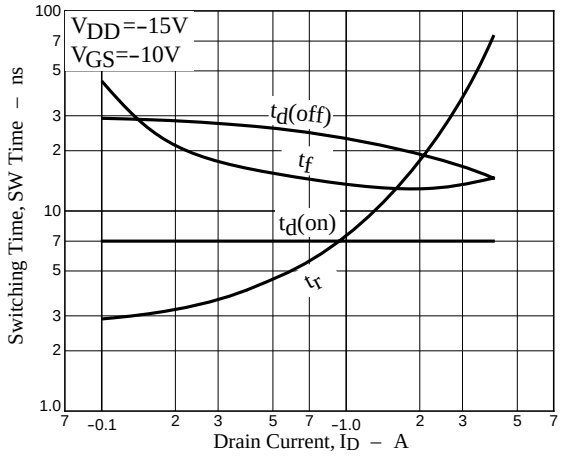
Ciss,Coss,Crss – V_{DS}



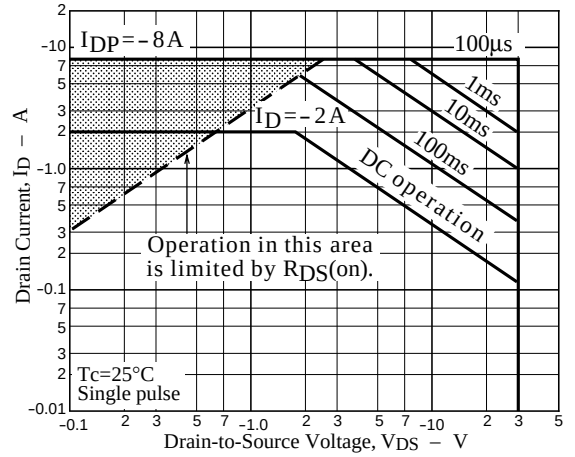
V_{GS} – Qg



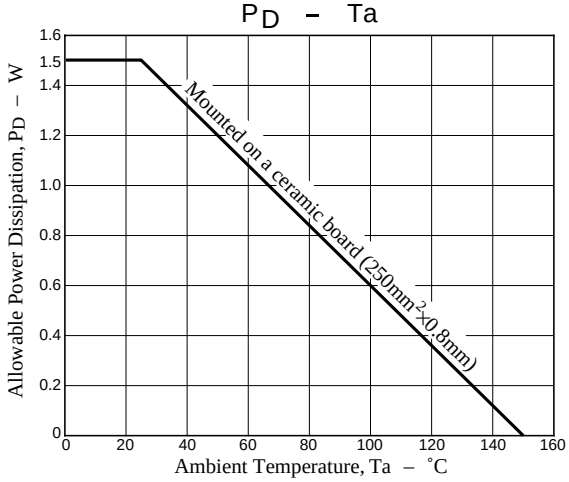
SW Time – I_D



A S O



P_D – Ta



P_D – Tc