

2SJ598-ZK

P-Channel Power [MOS FET](#)

-60V, -12A, 130mΩ

R07DS1587EJ0200

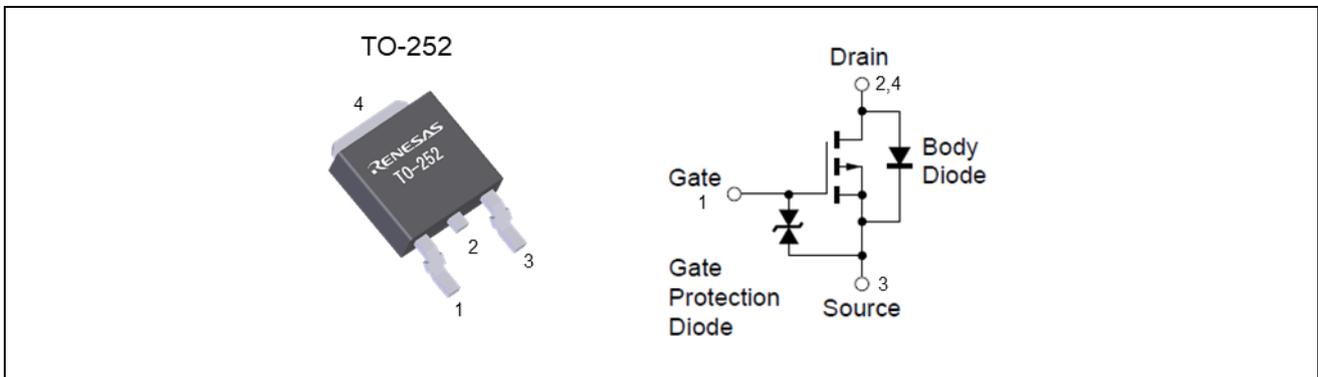
Rev.2.00

Feb.3.2025

Features

- Low on-state resistance
RDS(on)1 = 130 mΩ MAX. (VGS = -10 V, ID = -6 A)
RDS(on)2 = 190 mΩ MAX. (VGS = -4.0 V, ID = -6 A)
- Low Ciss: Ciss = 720 pF TYP.
- Built-in gate protection diode
- Applications : For switching

Outline



Absolute Maximum Ratings

(T_j=25°C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DSS}	-60	V
Gate to Source Voltage	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)} ^{Notes1,2,5}	±12	A
Drain Current (pulse)	I _{D(pulse)} ^{Notes1,3,5}	±30	A
Power Dissipation T _c = 25°C	P _D ^{Notes5}	23	W
Power Dissipation T _a = 25°C	P _D ^{Notes5}	1.0	W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55 to 150	°C
Single Avalanche Current	I _{AS} ^{Notes4}	-12	A
Single Avalanche Energy	E _{AS} ^{Notes4}	14.4	mJ

Thermal Resistance

Item	Symbol	Max	Unit
Junction to Case Thermal Resistance	R _{th(j-c)} ^{Notes5}	5.43	°C/W
Junction to Ambient Thermal Resistance	R _{th(j-a)} ^{Notes5}	125	°C/W

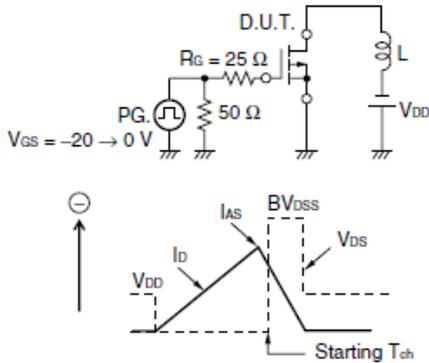
Electrical Characteristics

(T_j=25°C unless otherwise notice.)

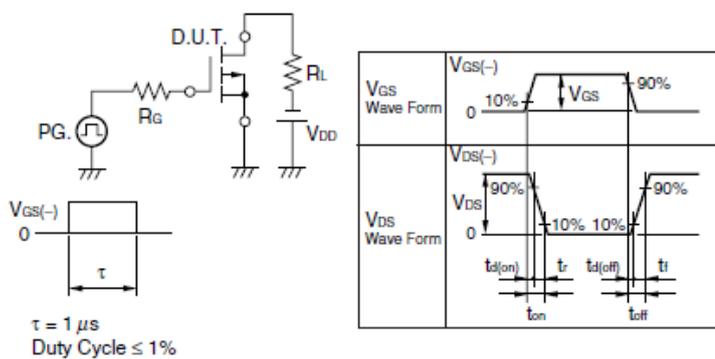
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	-1.5	-2.0	-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs}	5	11	—	S	V _{GS} = -10 V, I _D = -6 A
Drain to Source On-state Resistance	R _{DS(on)}	—	102	130	mΩ	V _{GS} = -10 V, I _D = -6 A
	R _{DS(on)}	—	131	190	mΩ	V _{GS} = -4.0 V, I _D = -6 A
Input Capacitance	C _{iss}	—	720	—	pF	V _{DS} = -10 V V _{GS} = 0 V f = 1 MHz
Output Capacitance	C _{oss}	—	150	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	50	—	pF	
Turn-on Delay Time	t _{d(on)}	—	7	—	ns	V _{DD} = -30 V I _D = -6 A
Rise Time	t _r	—	4	—	ns	
Turn-off Delay Time	t _{d(off)}	—	35	—	ns	V _{GS} = -10 V R _G = 0 Ω
Fall Time	t _f	—	10	—	ns	
Total Gate Charge	Q _g	—	15	—	nC	V _{DD} = -48 V V _{GS} = -10 V
Gate to Source Charge	Q _{gs}	—	3	—	nC	
Gate to Drain Charge	Q _{gd}	—	4	—	nC	I _D = -12 A
Body Diode Forward Voltage	V _{F(S-D)}	—	0.98	—	V	I _F = 12 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	50	—	ns	I _F = 12 A, V _{GS} = 0 V di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}	—	100	—	nC	

- Notes
1. T_C = 25°C
 2. Value is limited by overall system design including PCB
 3. PW ≤ 10 μs
 4. L = 100 μH, V_{DD} = -30 V, V_{GS} = -20 → 0 V, R_G = 25 Ω
 5. Defined by design. Not subject to production test.

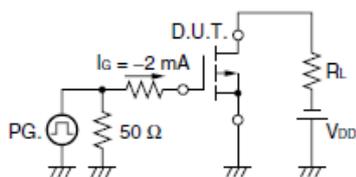
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

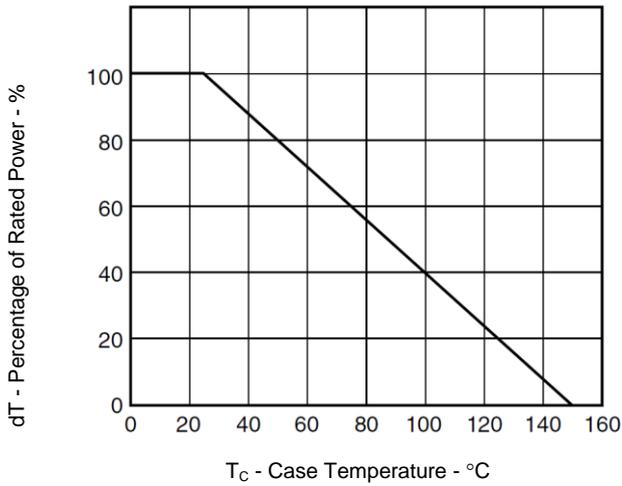


TEST CIRCUIT 3 GATE CHARGE

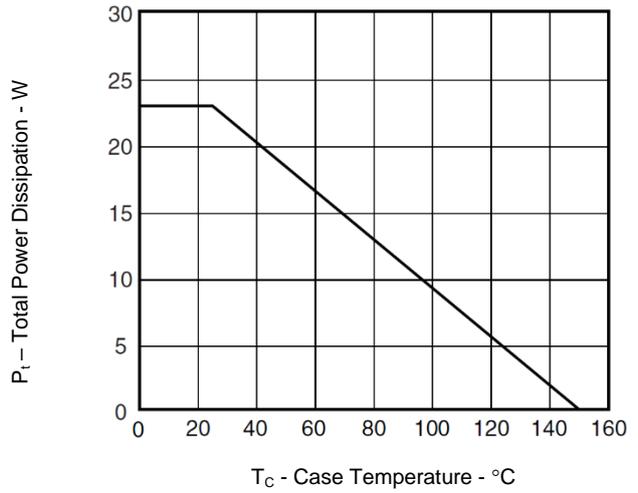


Typical Characteristics

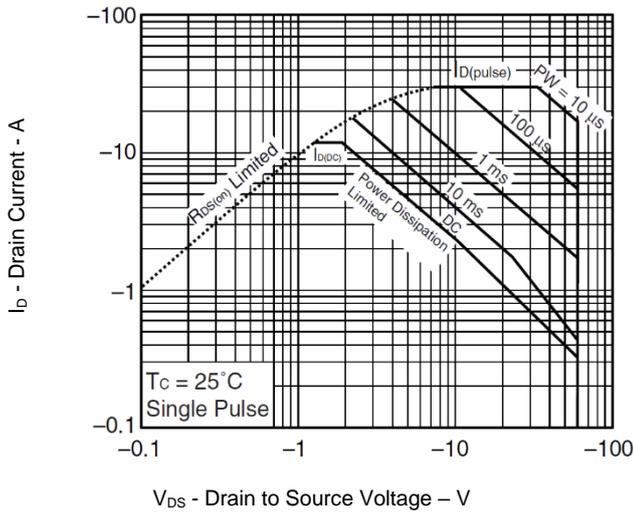
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



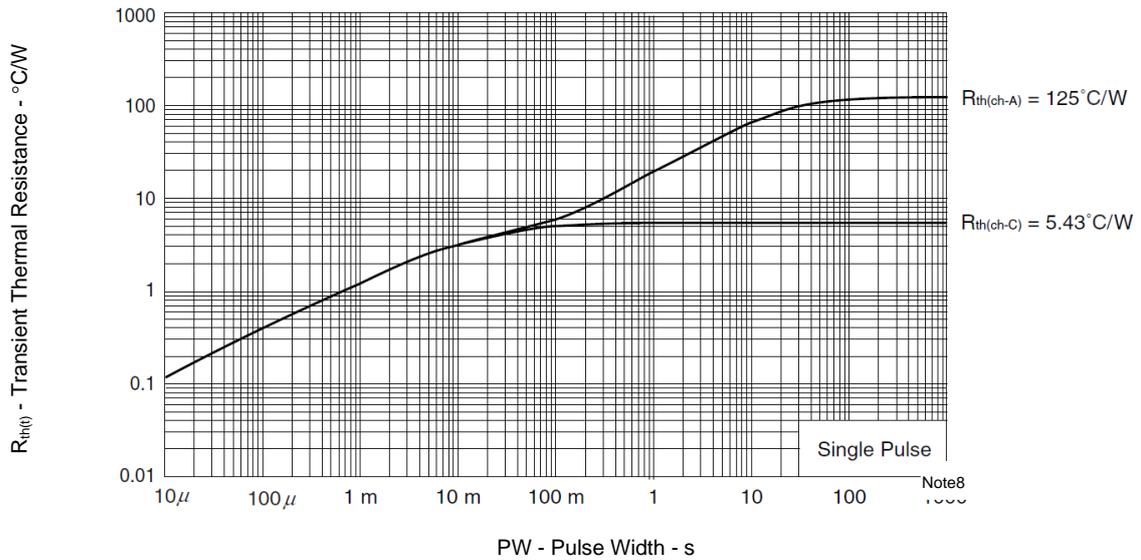
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



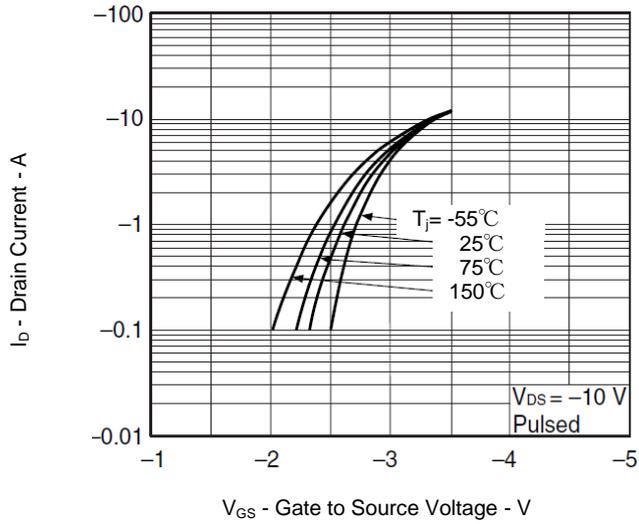
FORWARD BIAS SAFE OPERATING AREA



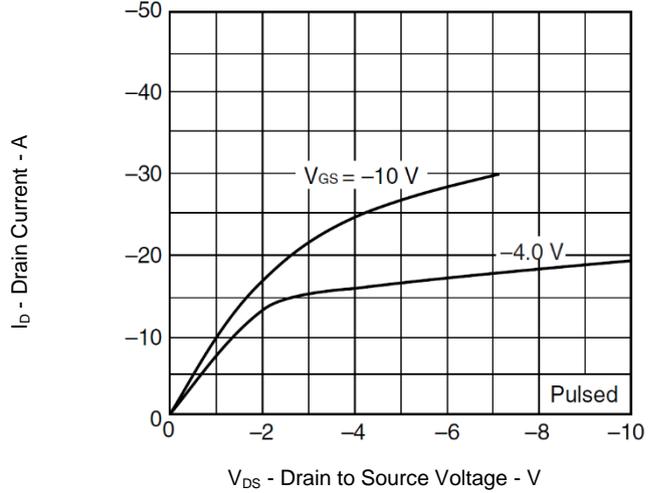
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



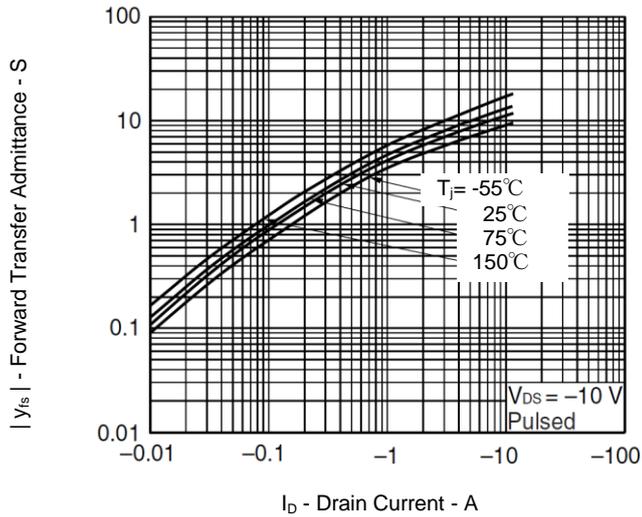
FORWARD TRANSFER CHARACTERISTICS



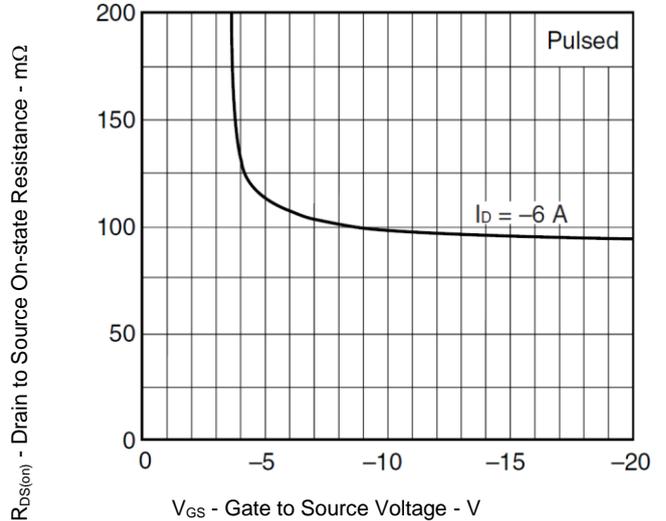
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



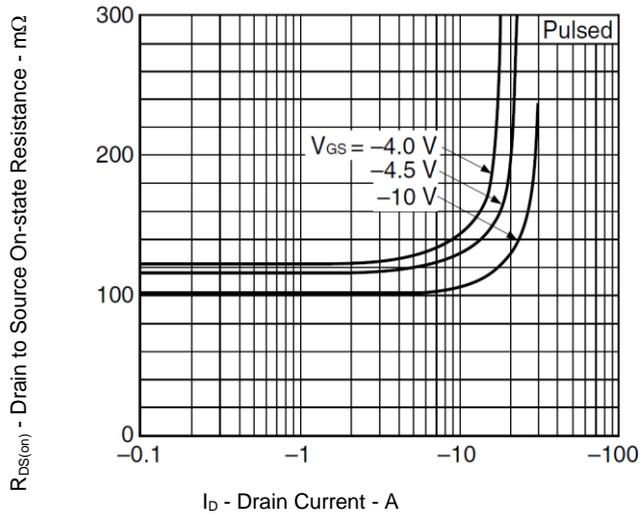
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



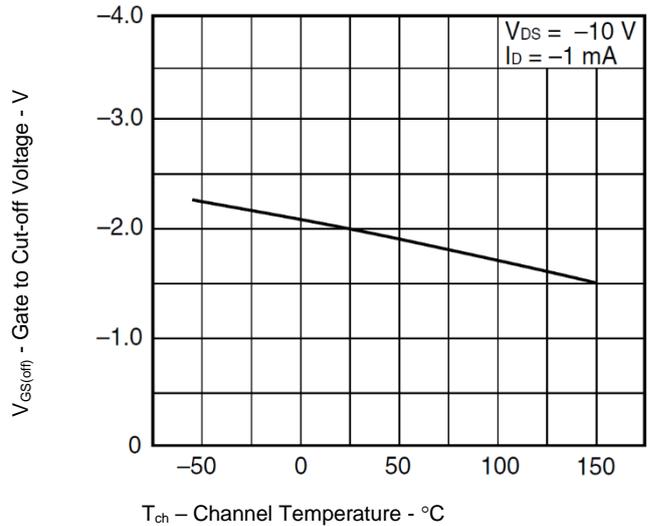
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

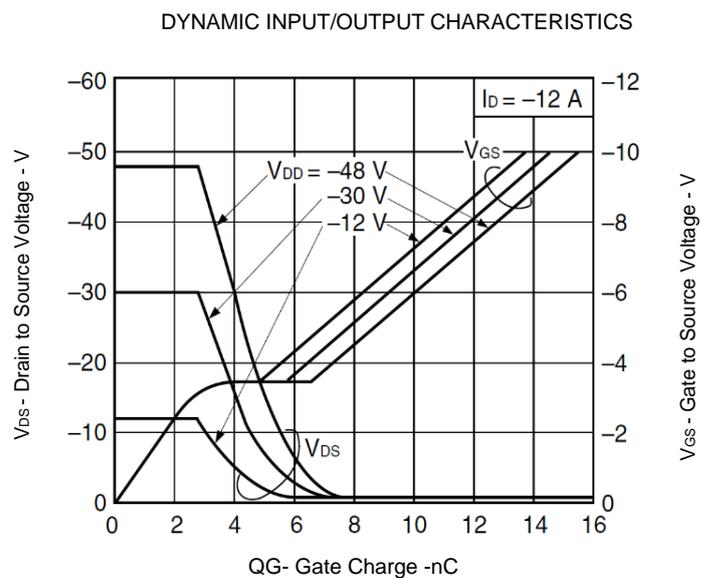
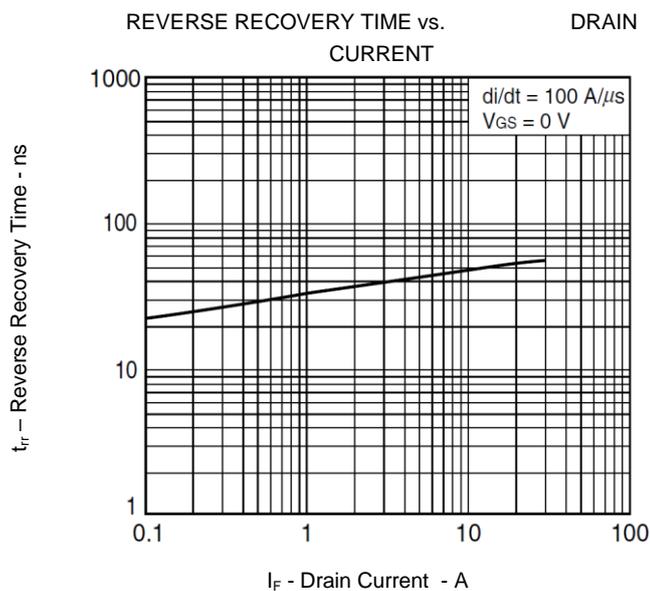
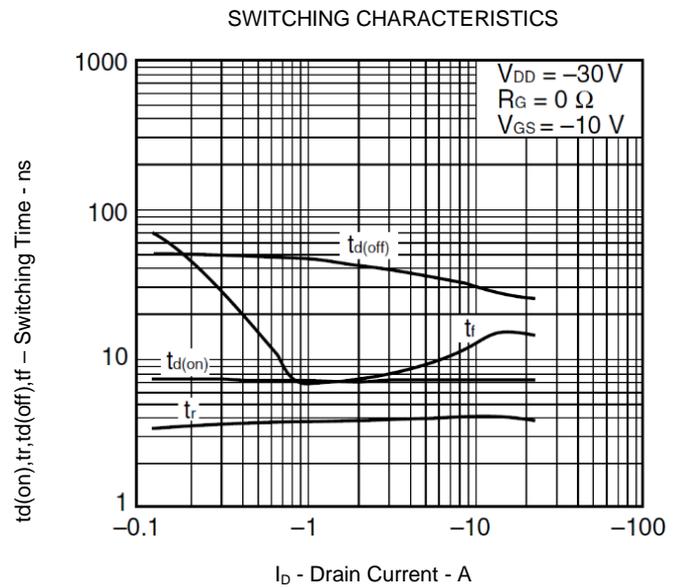
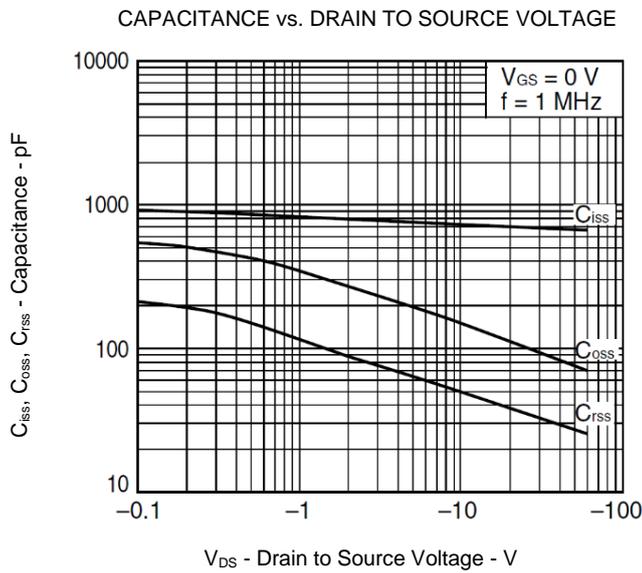
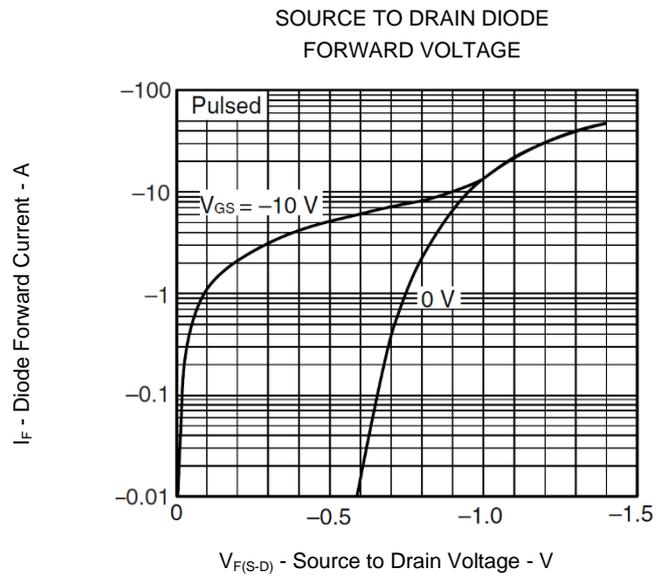
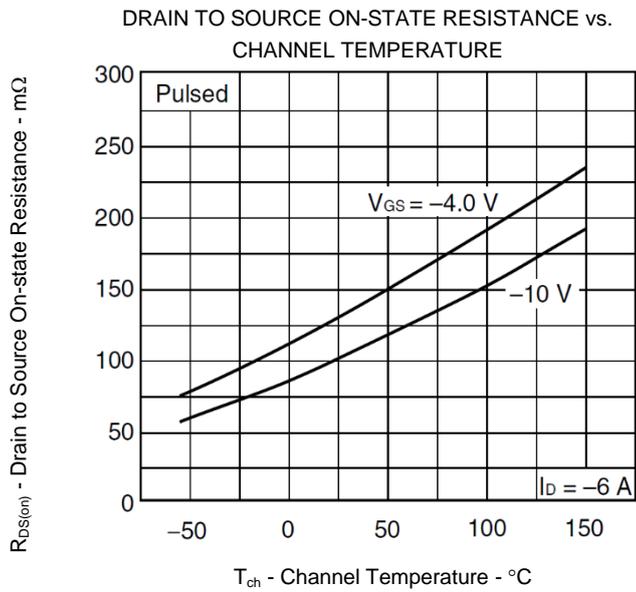


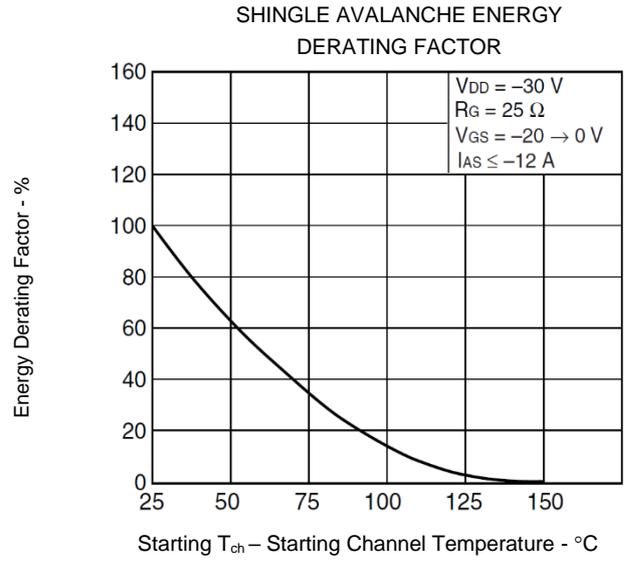
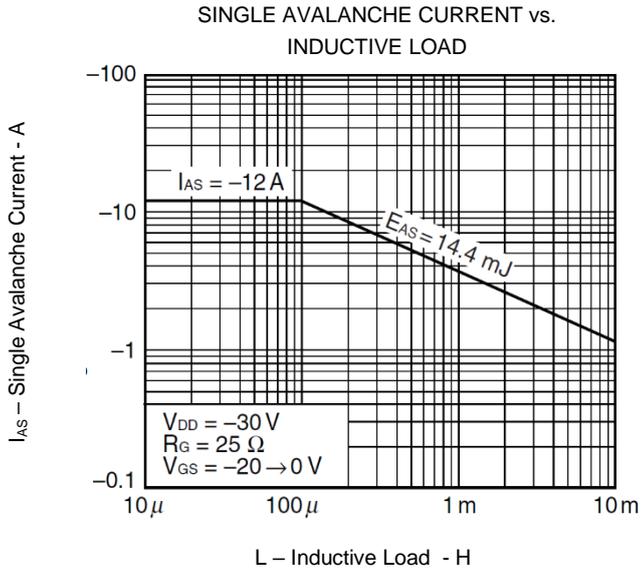
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

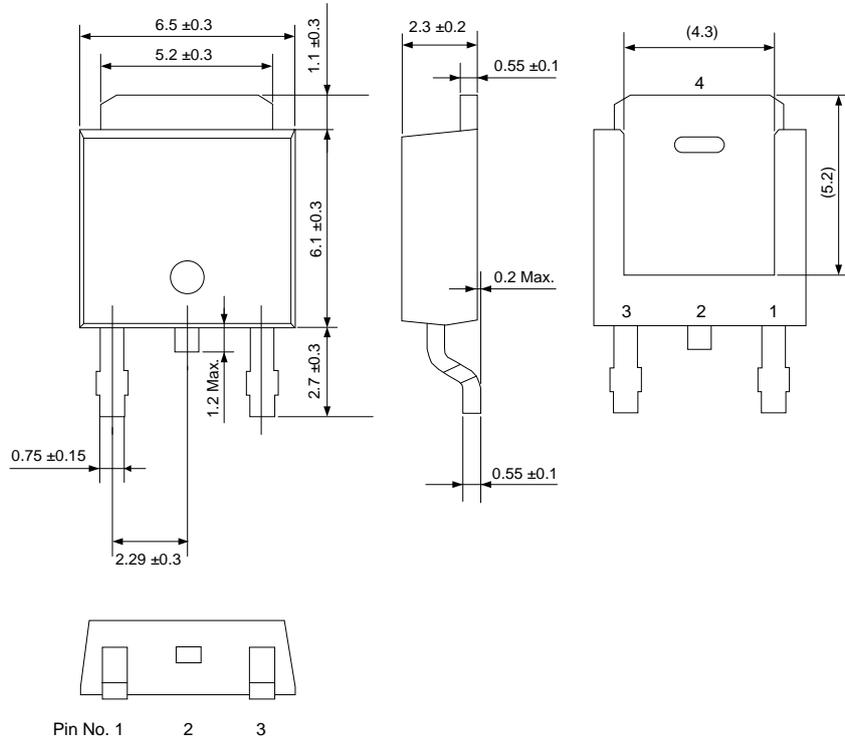




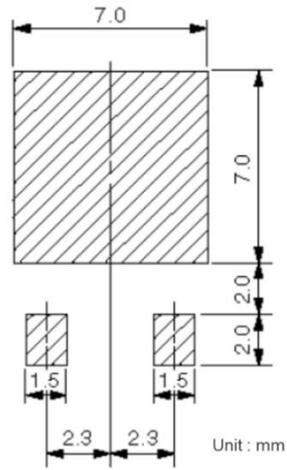


Package Dimensions (Unit : mm)

Package Name	JEITA Package Code	JEDEC Code	RENESAS Code	Previous Code	MASS (Typ) [g]
TO-252	—	TO-252	PRSS0004ZK-A	TO-252A	0.32



Mount Pad



Notice The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook.

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Revision History

Rev.	Date	Description	
		Page	Summary
-	Aug 2006	-	Previous No. D14656EJ5V0DS00
2.00	Feb 3 , 2025	7	Changed Package Dimensions