

**NEC****MOS FIELD EFFECT TRANSISTOR  
2SJ649****SWITCHING  
P-CHANNEL POWER MOS FET****DESCRIPTION**

The 2SJ649 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

**FEATURES**

- Low on-state resistance:
  - $R_{DS(on)1} = 48 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -10 \text{ A)}$
  - $R_{DS(on)2} = 75 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -10 \text{ A)}$
- Low input capacitance:
  - $C_{iss} = 1900 \text{ pF TYP. (} V_{DS} = -10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Built-in gate protection diode

**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )**

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-60	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\mp 20$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\mp 70$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_T$	25	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	-20	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	40	mJ

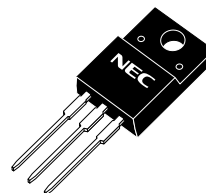
**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = -30 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = -20 \rightarrow 0 \text{ V}$

**ORDERING INFORMATION**

PART NUMBER	PACKAGE
2SJ649	Isolated TO-220

(Isolated TO-220)



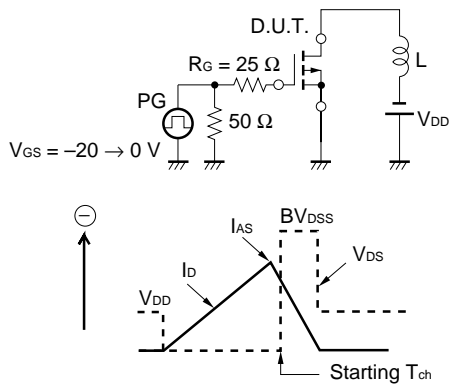
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

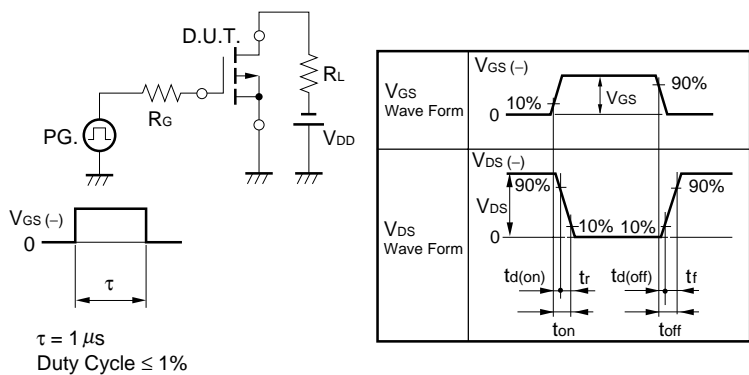
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.5	-2.0	-2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -10 A	10	20		S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A		38	48	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -10 A		47	75	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		1900		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		350		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		140		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, I <sub>D</sub> = -10 A		10		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -10 V		10		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		73		ns
Fall Time	t <sub>f</sub>			17		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -48 V		38		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V		7		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -20 A		10		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		0.95		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		49		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		100		nC

**Note** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

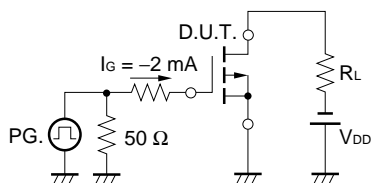
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

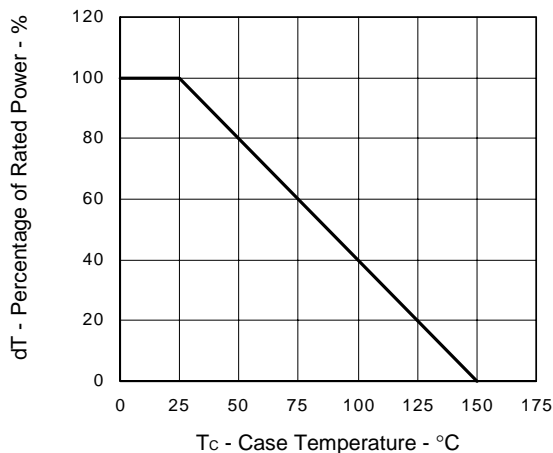


**TEST CIRCUIT 3 GATE CHARGE**

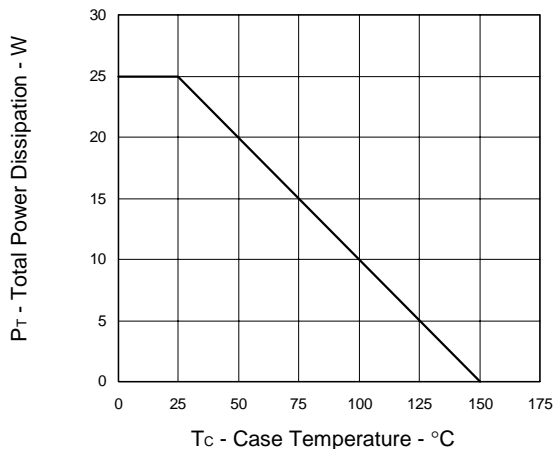


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

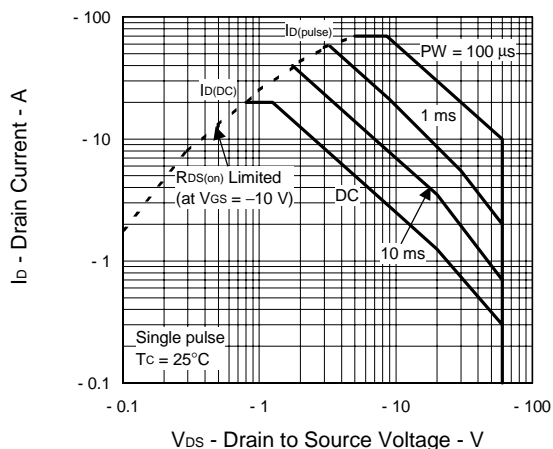
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



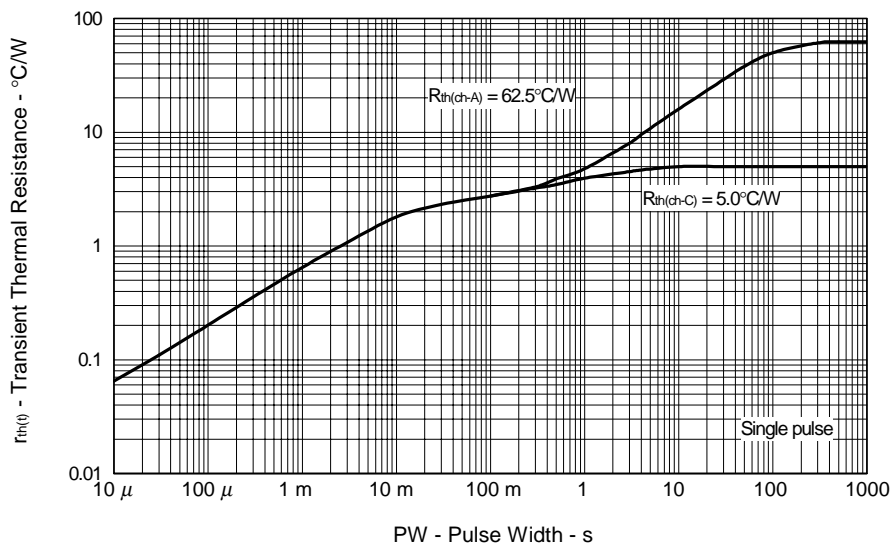
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



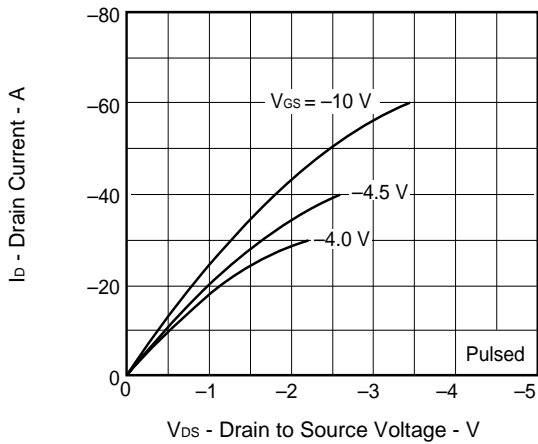
FORWARD BIAS SAFE OPERATING AREA



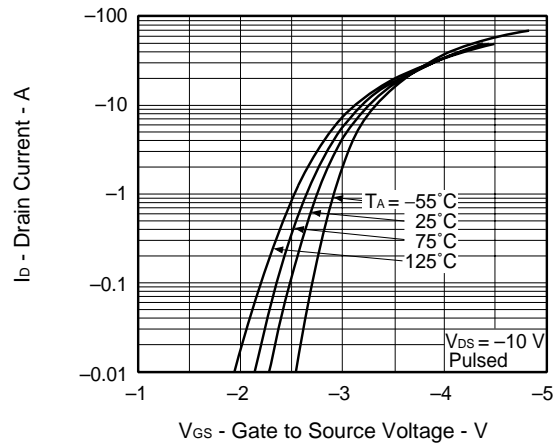
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



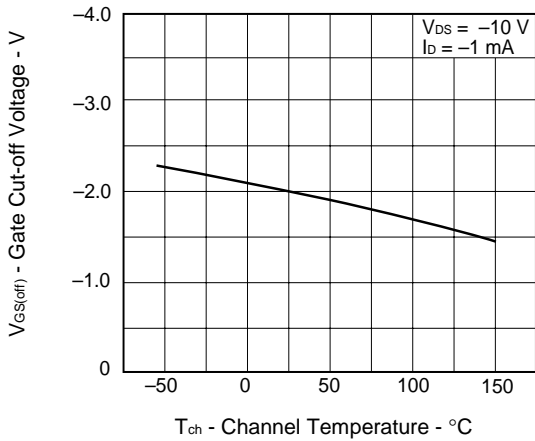
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



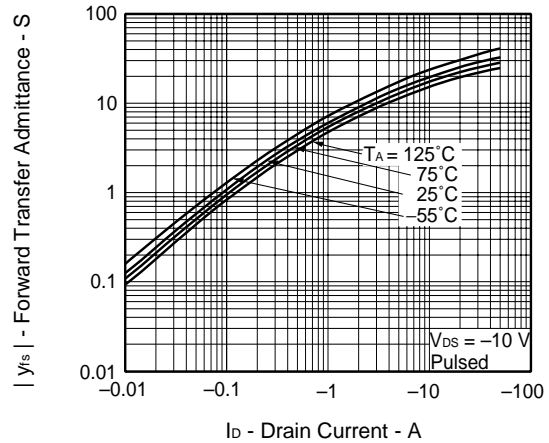
FORWARD TRANSFER CHARACTERISTICS



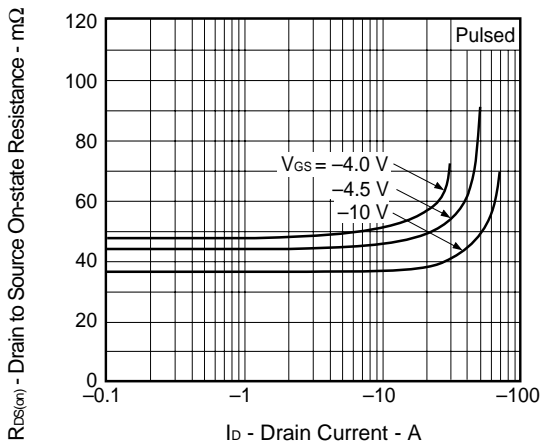
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



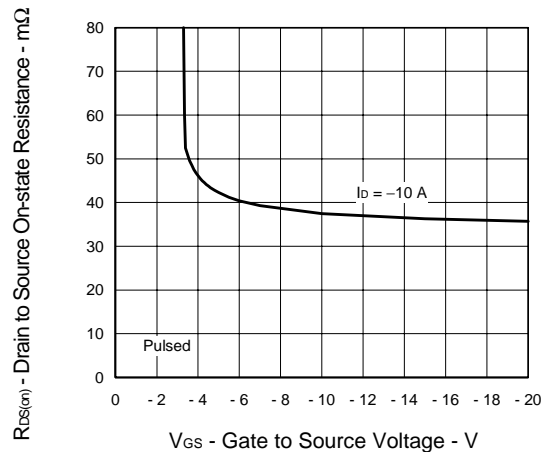
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



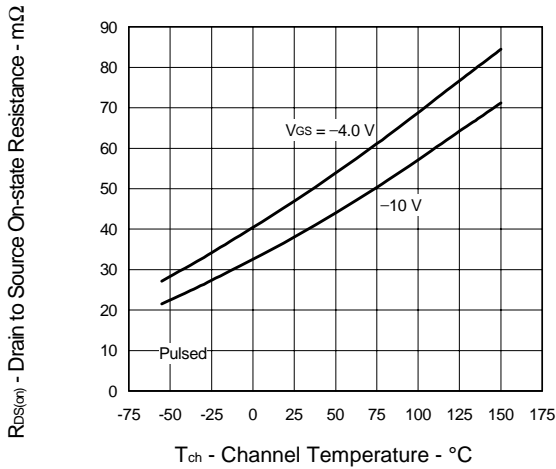
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



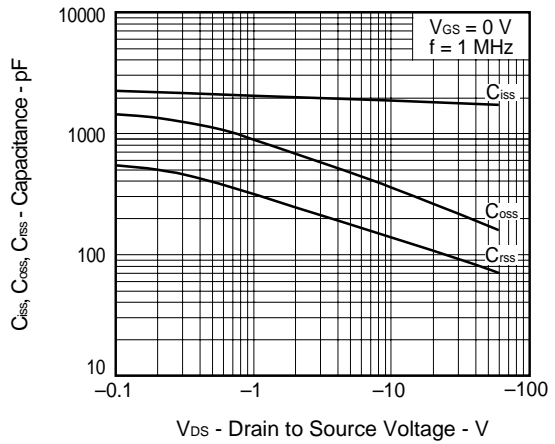
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



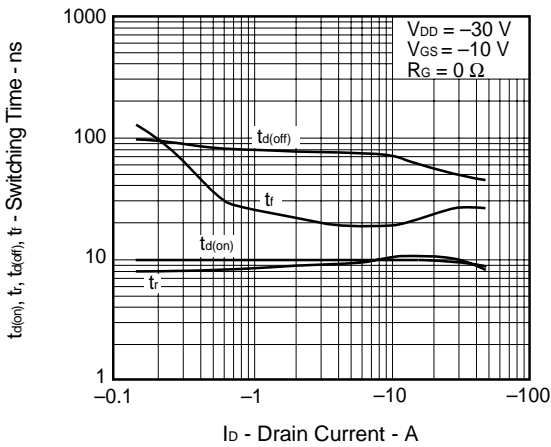
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



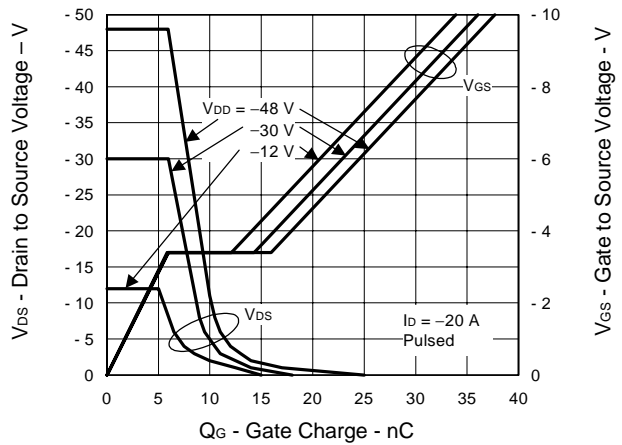
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



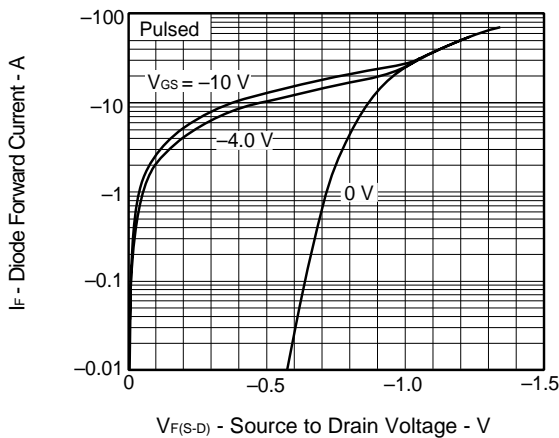
SWITCHING CHARACTERISTICS



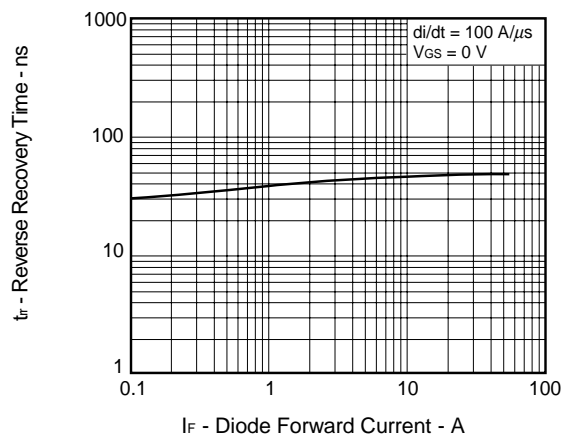
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



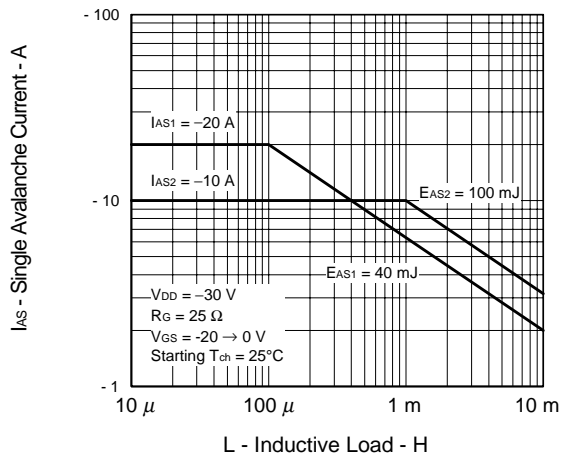
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



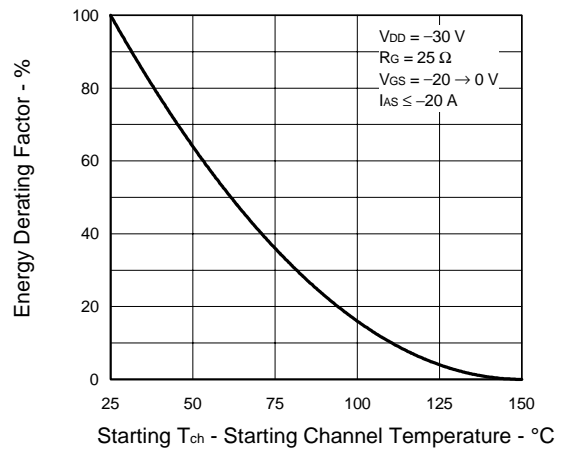
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

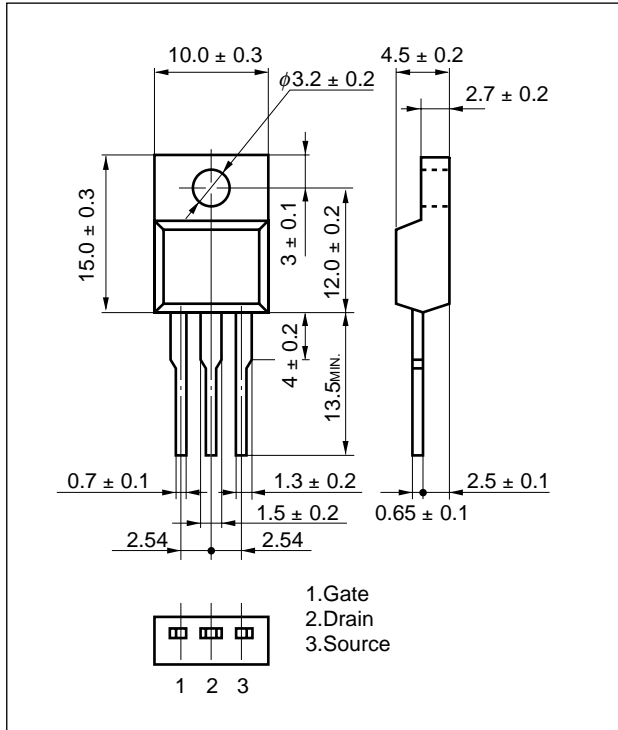


SINGLE AVALANCHE ENERGY DERATING FACTOR

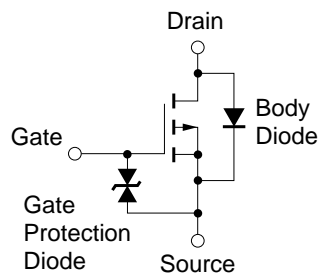


PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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