NEC

MOS FIELD EFFECT POWER TRANSISTOR
2SK1283

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1283 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance

  $R_{DS(on)} \leqq 0.18\ \Omega$ (V_{GS} = 10 V, I_D = 2 A)

  $R_{DS(on)} \leqq 0.24\ \Omega$ (V_{GS} = 4 V, I_D = 2 A)

- Low C_{iss} C_{iss} = 500 pF TYP.
- Built-in G-S Gate Protection Diode
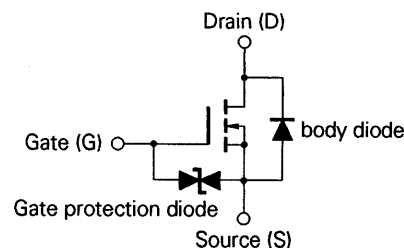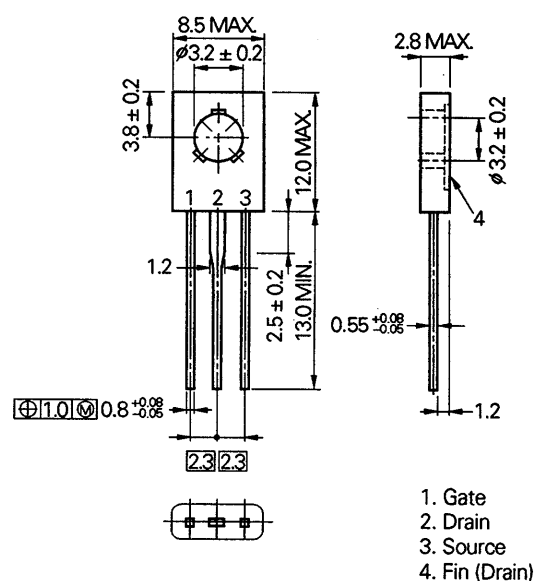
QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±3.0	A
Drain Current (pulse)	$I_{D(pulse)}$*	±12	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	20	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	1.3	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* PW $\leqq$ 10 μs, Duty Cycle $\leqq$ 1 %

PACKAGE DIMENSIONS
(in millimeters)

1. Gate
2. Drain
3. Source
4. Fin (Drain)

Drain (D)

Gate (G)

body diode

Gate protection diode

Source (S)

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

| CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.15	0.18	Ω	V_{GS} = 10 V, I_D = 2 A
Drain to Source On-state Resistance	$R_{DS(on)}$		0.18	0.24	Ω	V_{GS} = 4.0 V, I_D = 2 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$|y_{fs}|$	2.4			S	V_{DS} = 10 V, I_D = 2 A
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 60 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ± 20 V, V_{DS} = 0
Input Capacitance	C_{iss}		500		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		200		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		40		pF	f = 1 MHz
Turn-On Delay Time	$t_{d(on)}$		40		ns	$V_{GS(on)}$ = 10 V
Rise Time	t_r		100		ns	V_{DD} = 30 V
Turn-Off Delay Time	$t_{d(off)}$		550		ns	I_D = 2 A, R_G = 10 Ω
Fall Time	t_f		200		ns	R_L = 15 Ω
Total Gate Charge	Q_G		13		nC	V_{GS} = 10 V
Gate to Source Charge	Q_{GS}		3		nC	I_D = 3 A
Gate to Drain Charge	Q_{GD}		3		nC	V_{DD} = 48 V
Diode Forward Voltage	V_{SD}		0.9		V	I_{SD} = 3 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		140		ns	I_F = 3 A, V_{GS} = 0
Reverse Recovery Charge	Q_{rr}		700		nC	di/dt = 50 A/μs

Test Circuit 1: Switching Time
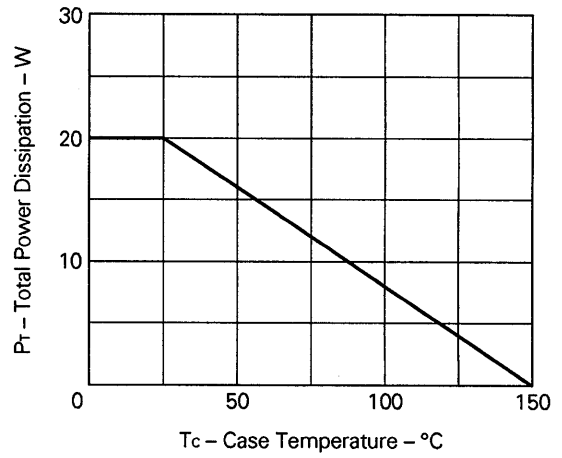

τ = 1 μs
Duty Cycle ≦ 1 %
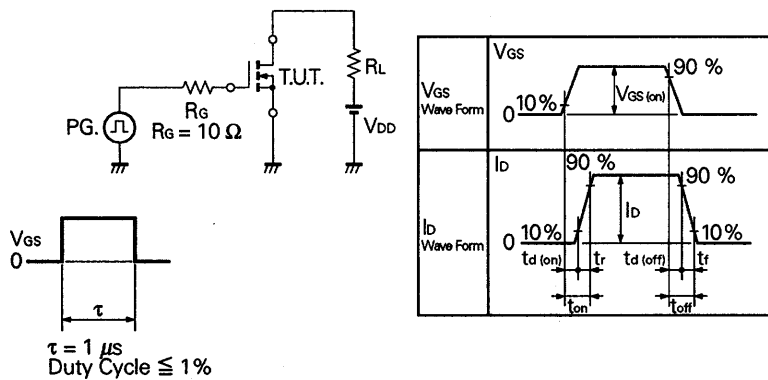
Test Circuit 2: Gate Charge
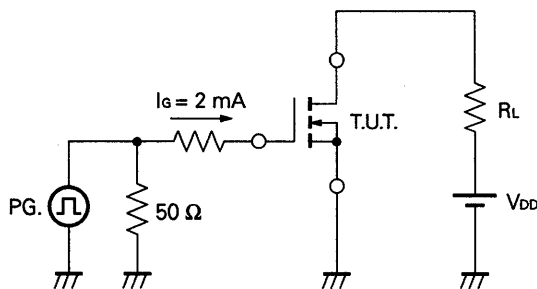
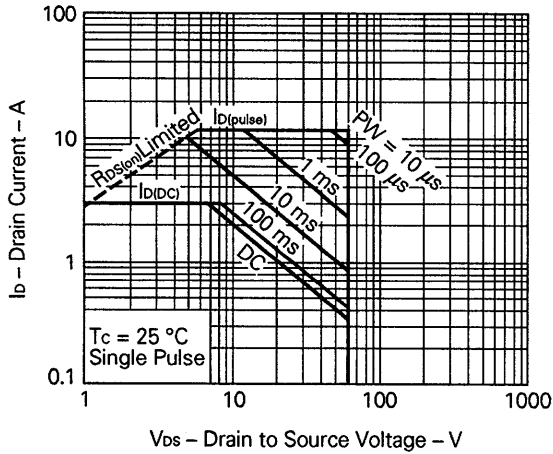## TYPICAL CHARACTERISTICS (T$_a$ = 25 °C)
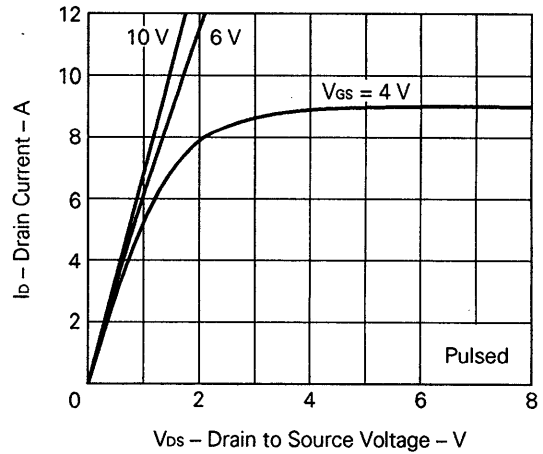
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA
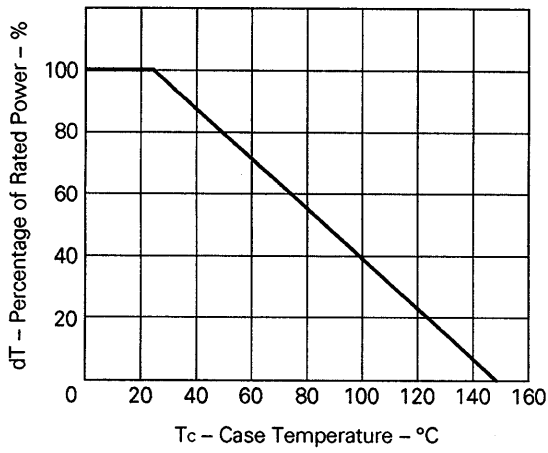
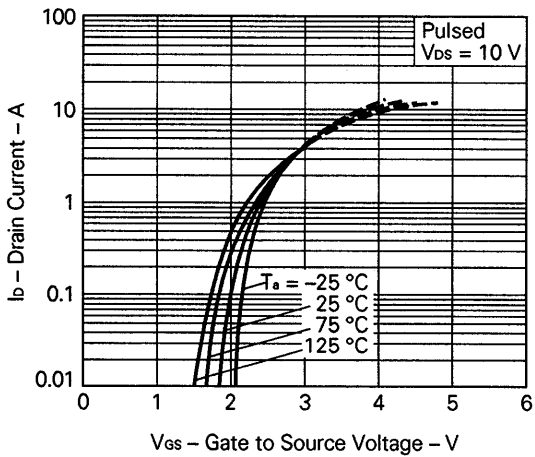TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE
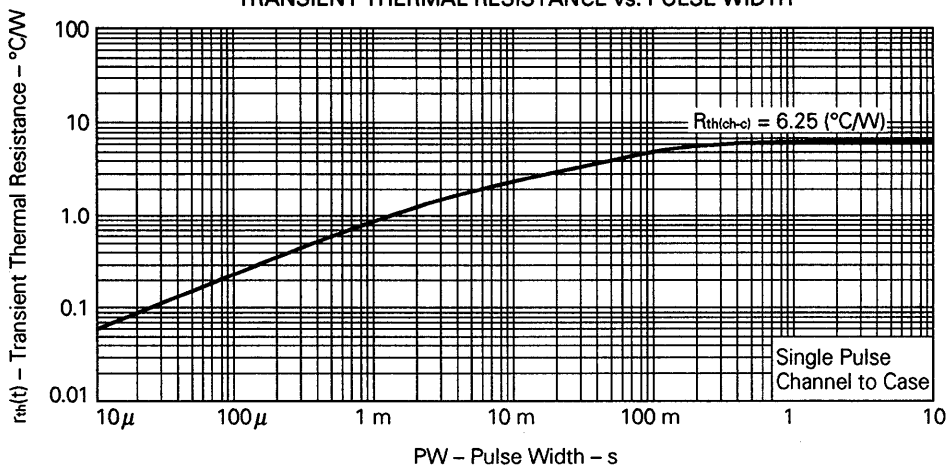
FORWARD BIAS SAFE OPERATING AREA

DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

TRANSFER CHARACTERISTICS
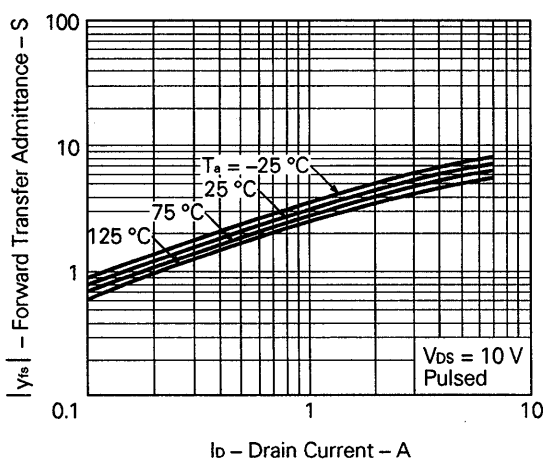
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TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

$R_{th(ch-c)}$ = 6.25 (°C/W)

Single Pulse
Channel to Case

$r_{th}(t)$ – Transient Thermal Resistance – °C/W

PW – Pulse Width – s

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

T_a = –25 °C
25 °C
75 °C
125 °C

V_{DS} = 10 V
Pulsed

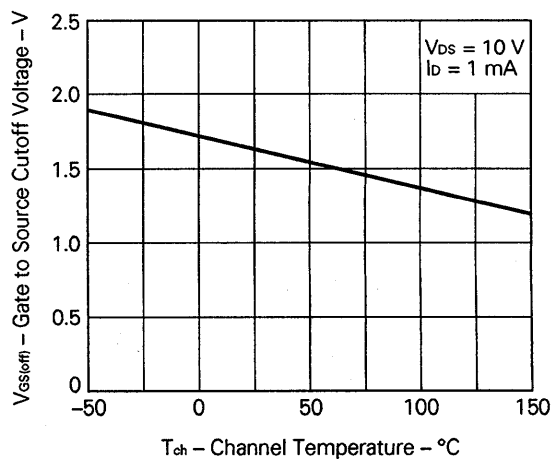$|y_{fs}|$ – Forward Transfer Admittance – S

I_D – Drain Current – A

DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

Pulsed

I_D = 3 A
2 A
0.6 A

V_{DS} – Drain to Source Voltage – V

V_{GS} – Gate to Source Voltage – V
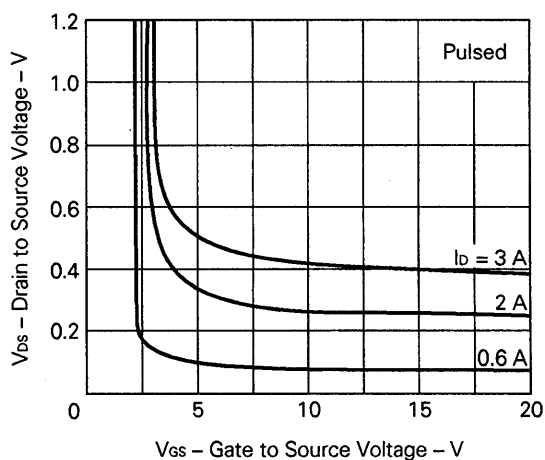
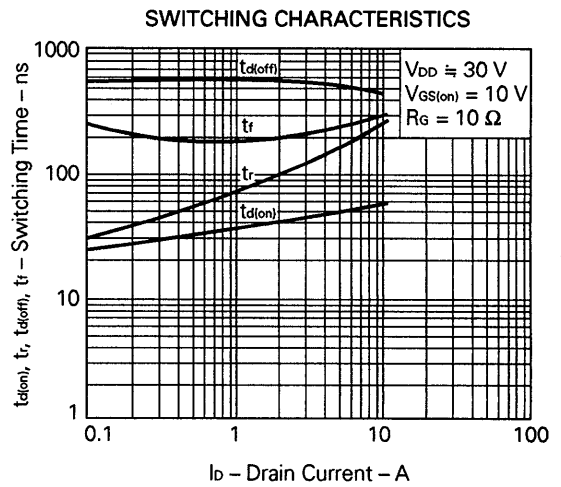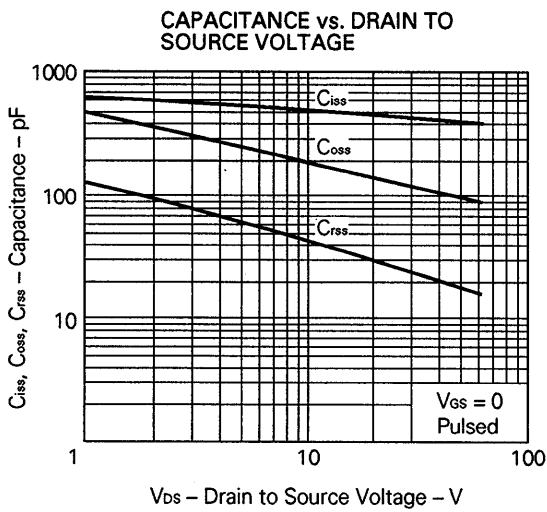## DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

V_{GS} = 4 V
10 V

Pulsed

$R_{DS(on)}$ – Drain to Source On-State Resistance – Ω

I_D – Drain Current – A
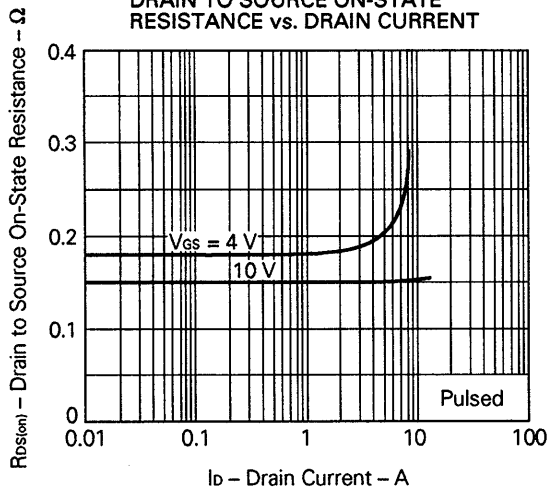
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

V_{DS} = 10 V
I_D = 1 mA

$V_{GS(off)}$ – Gate to Source Cutoff Voltage – V

T_{ch} – Channel Temperature – °C

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DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

$R_{DS(on)}$ – Drain to Source On-State Resistance – Ω

$V_{GS} = 4\,V$
$10\,V$

Pulsed
$I_D = 2\,A$

T_{ch} – Channel Temperature – °C

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

I_{SD} – Diode Forward Current – A

Pulsed

$4\,V$ $V_{GS} = 0$

V_{SD} – Source to Drain Voltage – V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

C_{iss}, C_{oss}, C_{rss} – Capacitance – pF

C_{iss}
C_{oss}
C_{rss}

$V_{GS} = 0$
Pulsed

V_{DS} – Drain to Source Voltage – V

SWITCHING CHARACTERISTICS

$t_{d(on)}$, t_f, $t_{d(off)}$, t_r – Switching Time – ns

$t_{d(off)}$
t_f
t_r
$t_{d(on)}$

$V_{DD} \doteq 30\,V$
$V_{GS(on)} = 10\,V$
$R_G = 10\,\Omega$

I_D – Drain Current – A

DYNAMIC INPUT CHARACTERISTICS

V_{DS} – Drain to Source Voltage – V

V_{GS} – Gate to Source Voltage – V

$I_D = 3\,A$

V_{DS}
V_{GS}

$V_{DD} = 48\,V$
$30\,V$
$12\,V$

Q_g – Gate Charge – nC

REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

t_{rr} – Reverse Recovery Time – ns

$di/dt = 50\,A/\mu s$
$V_{GS} = 0$

I_F – Diode Forward Current – A

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Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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