

2SK1304-VB Datasheet

N-Channel 100-V (D-S) 175 °C MOSFET

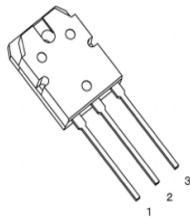
PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
100	0.0085 at V _{GS} = 10 V	100
	0.010 at V _{GS} = 6 V	85

FEATURES

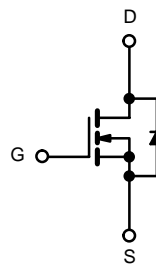
- TrenchFET[®] Power MOSFET
- 175 °C Maximum Junction Temperature
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT



TO-3P(N)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	100
		T _C = 125 °C	75 ^a
Pulsed Drain Current	I _{DM}	300	A
Avalanche Current	I _{AS}	75	
Single Pulse Avalanche Energy ^b	E _{AS}	280	mJ
Maximum Power Dissipation ^b	P _D	T _C = 25 °C (TO-220AB and TO-263)	250 ^c
		T _A = 25 °C (TO-263) ^d	3.75
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R _{thJA}	PCB Mount (TO-263) ^d	40
		Free Air (TO-220AB)	62.5
Junction-to-Case	R _{thJC}	0.6	°C/W

Notes:

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

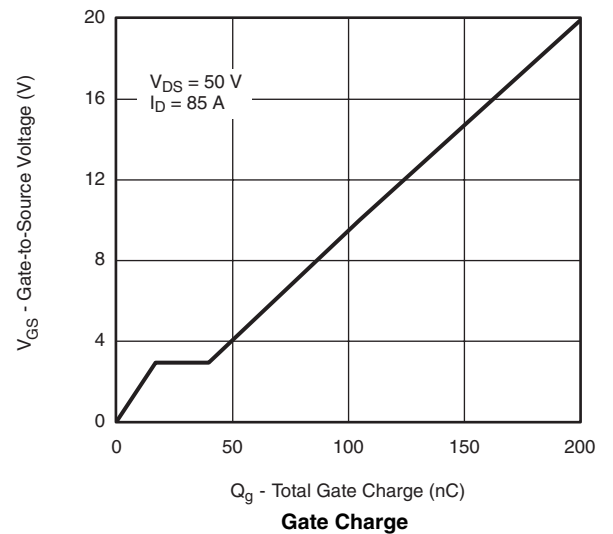
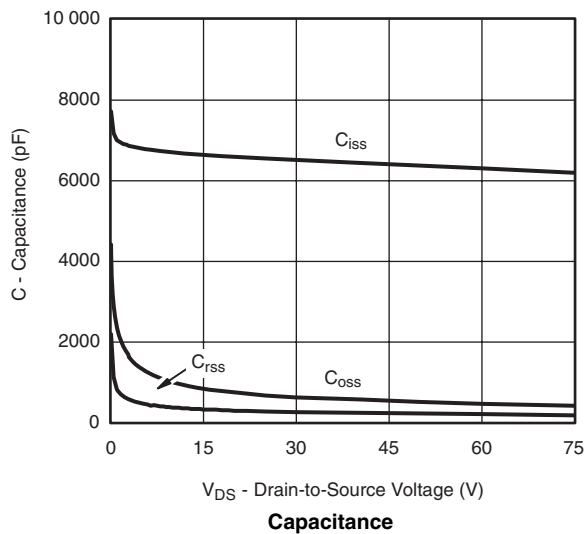
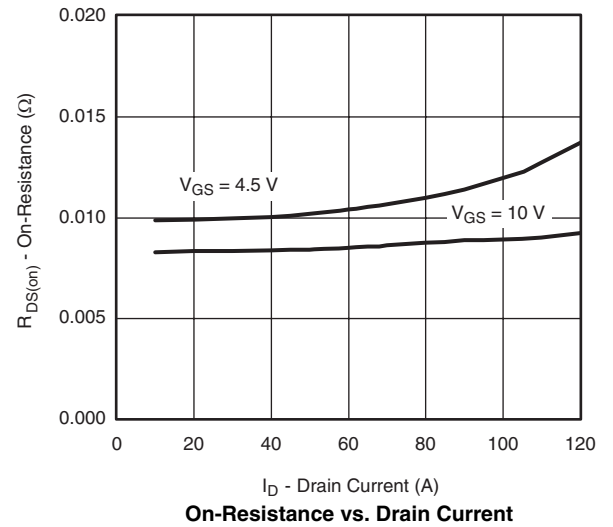
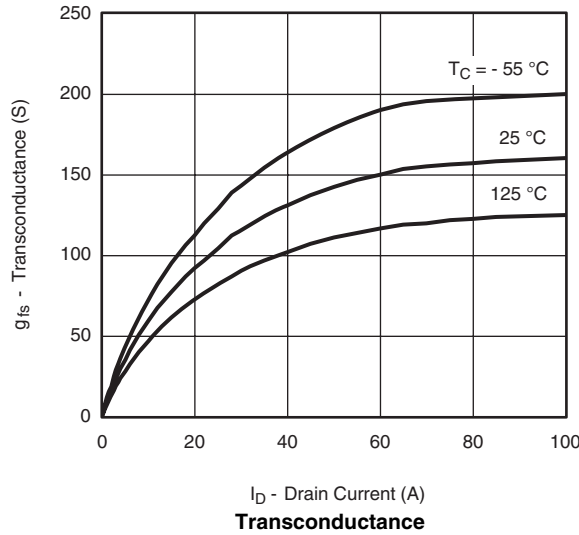
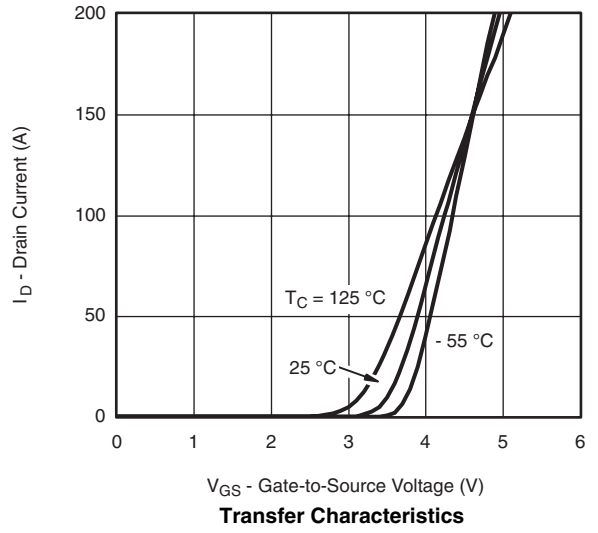
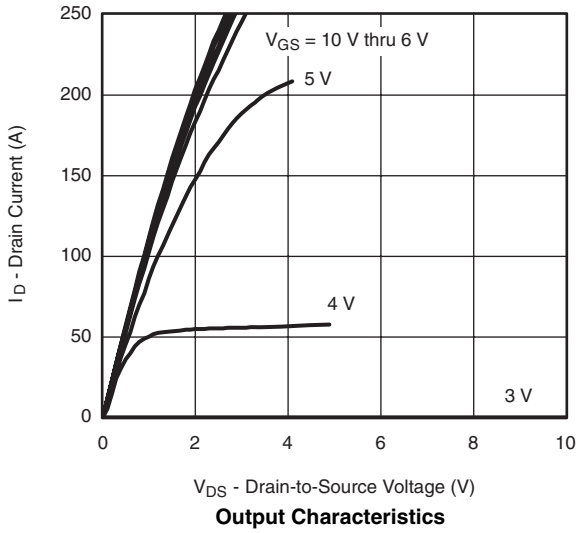
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		0.0085		Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.010		
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.017		
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175\text{ }^\circ\text{C}$		0.022		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	25			S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		6550		pF
Output Capacitance	C_{oss}			665		
Reverse Transfer Capacitance	C_{rss}			265		
Total Gate Charge ^c	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 85\text{ A}$		105	160	nC
Gate-Source Charge ^c	Q_{gs}			17		
Gate-Drain Charge ^c	Q_{gd}			23		
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong 85\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		12	25	ns
Rise Time ^c	t_r			90	135	
Turn-Off Delay Time ^c	$t_{d(off)}$			55	85	
Fall Time ^c	t_f			130	195	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$ ^b						
Continuous Current	I_S				85	A
Pulsed Current	I_{SM}				240	
Forward Voltage ^a	V_{SD}	$I_F = 85\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		85	140	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			4.5	7	A
Reverse Recovery Charge	Q_{rr}			0.17	0.35	μC

Notes:

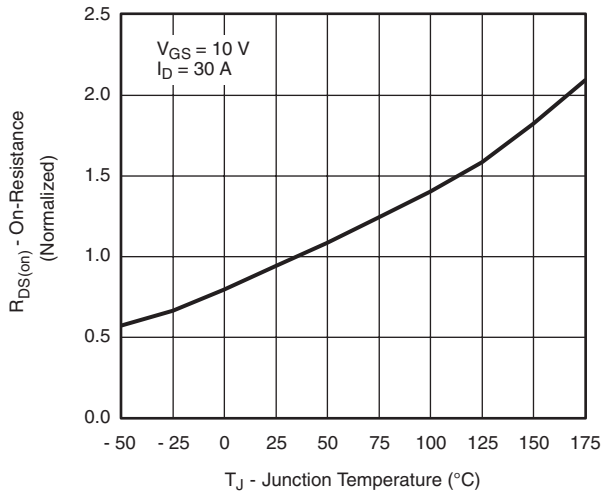
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

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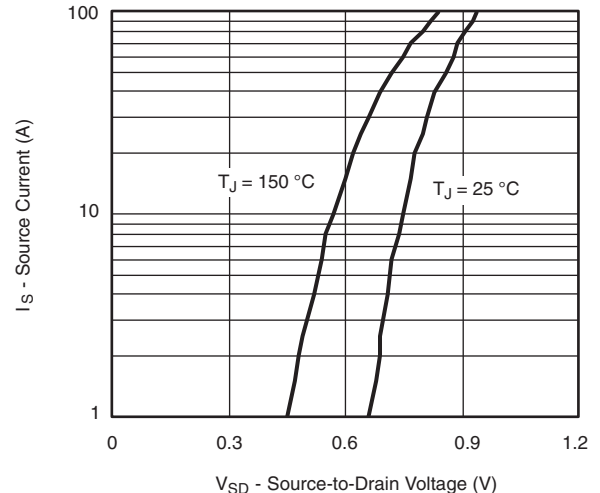
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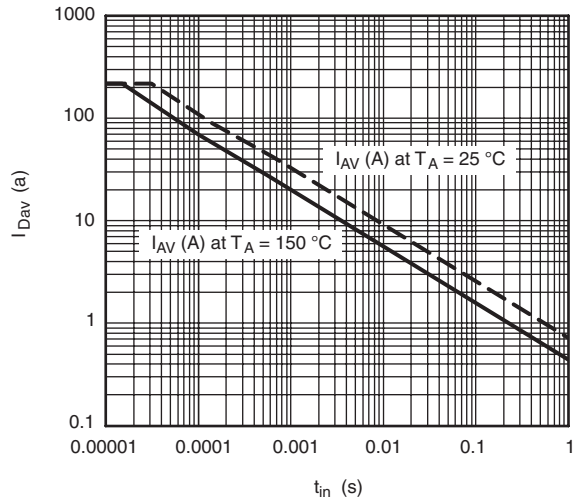
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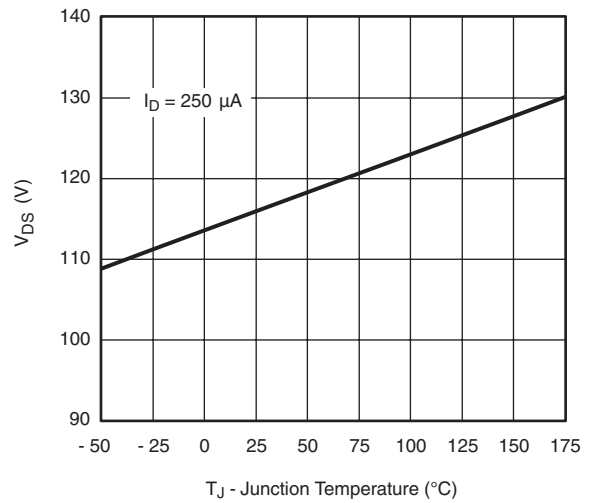
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

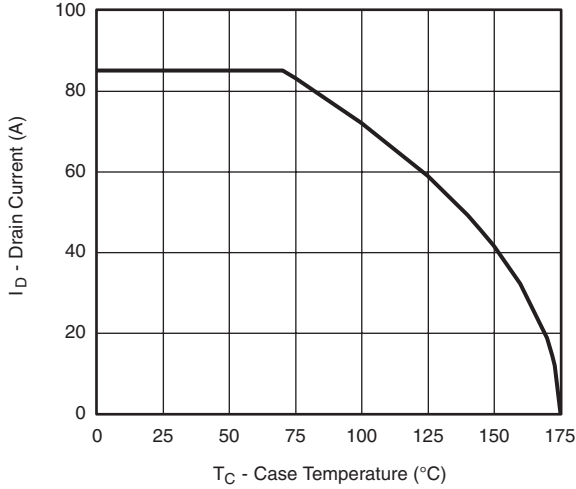


Avalanche Current vs. Time

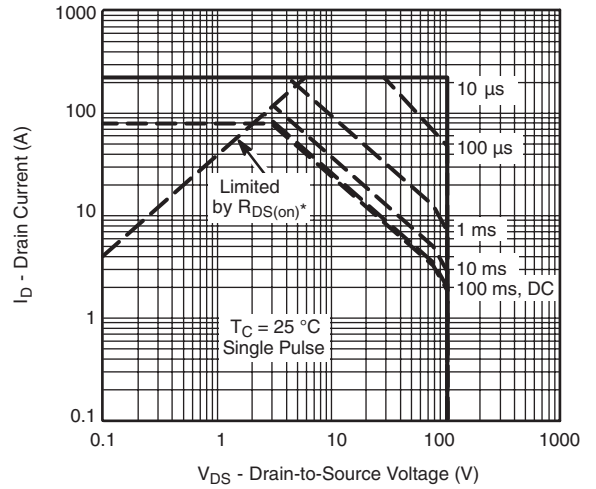


T_J - Drain-Source Breakdown vs. Junction-Temperature

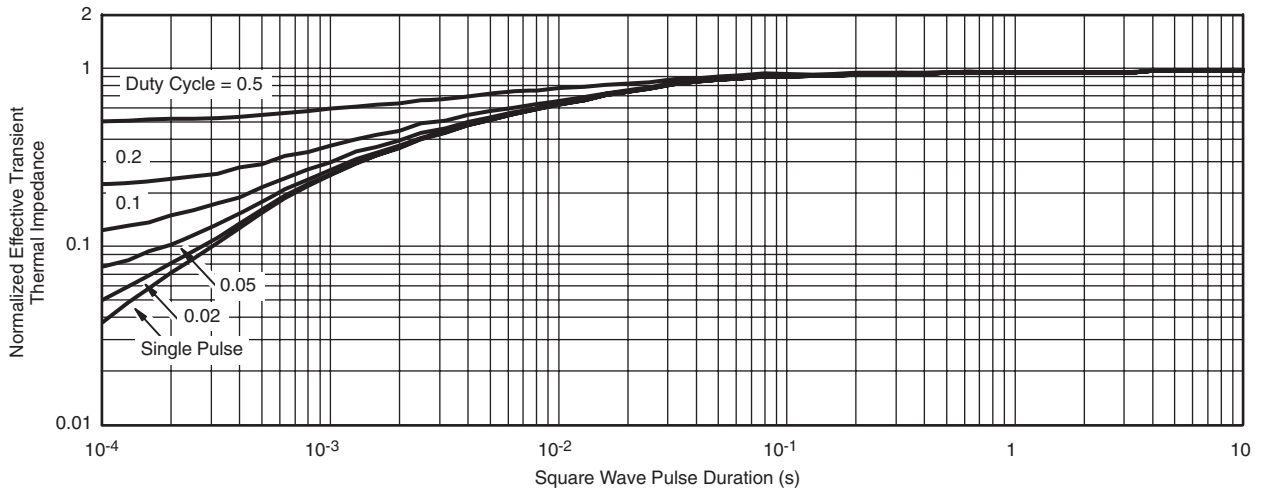
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

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